INTERNATIONAL SEARCH REPORT

national Application No
PCT/GB 99/01339

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L1/20 H04L7/033

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category '	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 975 634 A (SHOHET YUVAL) 4 December 1990 (1990-12-04) the whole document	1-15
A	EP 0 362 491 A (WANDEL & GOLTERMANN) 11 April 1990 (1990-04-11) the whole document	1-15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

' Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 July 1999	04/08/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Toumpoulidis, T

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 99/01339

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4975634 A	04-12-1990	NONE	
EP 0362491 A	11-04-1990	DE 3833486 C	03-08-1989
		DK 471789 A	02-04-1990
		JP 1948838 C	10-07-1995
		JP 2147866 A	06-06-1990
		JP 6077041 B	28-09-1994
		US 4974234 A	27-11-1990

09/674444

PATENT COOPERATION TREATY

CORRECTED VERSION

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

From the INTERNATIONAL BUREAU

To:

CALDERBANK, T., Roger
Mewburn Ellis
York House
23 Kingsway
London WC2B 6HP
ROYAUME-UNI

Date of mailing (day/month/year) 29 November 2000 (29.11.00)	
Applicant's or agent's file reference TRC/BP5764824	**IMPORTANT NOTIFICATION**
International application No. PCT/GB99/01339	**International filing date** (day/month/year) 29 April 1999 (29.04.99)

1. The following indications appeared on record concerning:

[X] the applicant [ ] the inventor [ ] the agent [ ] the common representative

Name and Address

WANDEL & GOLTERMANN
Eurotech House
Burrington Way
Plymouth
Devon PL5 3LZ
United Kingdom

State of Nationality | State of Residence

Telephone No.

Facsimile No.

Teleprinter No.

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[ ] the person [X] the name [ ] the address [ ] the nationality [ ] the residence

Name and Address

WAVETEK WANDEL GOLTERMANN PLYMOUTH LIMITED
Eurotech House
Burrington Way
Plymouth
Devon PL5 3LZ
United Kingdom

State of Nationality | State of Residence

Telephone No.

Facsimile No.

Teleprinter No.

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[X] the International Preliminary Examining Authority
[ ] the designated Offices concerned
[X] the elected Offices concerned
[ ] other:

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Anman QIU
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

Form PCT/IB/306 (March 1994)

003688993

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 22 December 1999 (22.12.99)	
International application No. PCT/GB99/01339	**Applicant's or agent's file reference** TRC/BP5764824
International filing date (day/month/year) 29 April 1999 (29.04.99)	**Priority date** (day/month/year) 01 May 1998 (01.05.98)
Applicant BREWER, Symon, Reuben	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

30 November 1999 (30.11.99)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Juan Cruz
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

Form PCT/IB/331 (July 1992)

3026669

Copy for the Elected Office (EO/US)

PCT/GB99/01339

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

To:

CALDERBANK, T., Roger
Mewburn Ellis
York House
23 Kingsway
London WC2B 6HP
ROYAUME-UNI

Date of mailing (day/month/year)
21 January 2000 (21.01.00)

Applicant's or agent's file reference
TRC/BP5764824

IMPORTANT NOTIFICATION

International application No.
PCT/GB99/01339

International filing date (day/month/year)
29 April 1999 (29.04.99)

1. The following indications appeared on record concerning:

[X] the applicant [ ] the inventor [ ] the agent [ ] the common representative

Name and Address
WANDEL & GOLTERMANN
Eurotech House
Burrington Way
Plymouth
Devon PL5 3LZ
United Kingdom

State of Nationality: GB
State of Residence: GB
Telephone No.:
Facsimile No.:
Teleprinter No.:

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[ ] the person [X] the name [ ] the address [ ] the nationality [ ] the residence

Name and Address
WAVETECK WANDEL GOLTERMANN
PLYMOUTH LIMITED
Eurotech House
Burrington Way
Plymouth
Devon PL5 3LZ
United Kingdom

State of Nationality: GB
State of Residence: GB
Telephone No.:
Facsimile No.:
Teleprinter No.:

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[X] the International Preliminary Examining Authority
[ ] the designated Offices concerned
[X] the elected Offices concerned
[ ] other:

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No.: (41-22) 740.14.35

Authorized officer
Athina Nickitas-Etienne

Telephone No.: (41-22) 338.83.38

09/674444

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty

For receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference (if desired) (12 characters maximum) TRC/BP5764824

Box No. I TITLE OF INVENTION JITTER MEASUREMENT

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

WANDEL & GOLDERMANN
EUROTECH HOUSE
BURRINGTON WAY
PLYMOUTH
DEVON
PL5 3LZ
GB

☐ This person is also inventor.

Telephone No.

Facsimile No.

Teleprinter No.

State *(that is, country) of nationality:* GB

State *(that is, country) of residence:* GB

This person is applicant for the purposes of: ☐ all designated States ☒ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

BREWER SYMON REUBEN
48 PEVERELL PARK ROAD
PEVERELL
PLYMOUTH
PL3 4NB
GB

This person is:

☐ applicant only

☒ applicant and inventor

☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country) of nationality:* GB

State *(that is, country) of residence:* GB

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☒ agent ☐ common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

CALDERBANK, T. ROGER and others
MEWBURN ELLIS
YORK HOUSE
23 KINGSWAY
LONDON WC2B 6HP
GB

Telephone No. 0117 9266411

Facsimile No. +44 171 240 9339

Teleprinter No. 22762 PATENT G

☐ Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Box No. V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked)*:

Regional

- ☐ AP — **ARIPO Patent:** GH Ghana, GM Gambia, KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SZ Swaziland, UG Uganda, ZW Zimbabwe, and any other State which is a Contracting State of the Harare Protocol and of the PCT
- ☐ EA — **Eurasian Patent:** AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakhstan, MD Republic of Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- ☒ EP — **European Patent:** AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, CY Cyprus, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT
- ☐ OA — **OAPI Patent:** BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, GW Guinea-Bissau, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)*

.....

National Patent *(if other kind of protection desired, specify on dotted line)*:

☐	AL	Albania	☐	LT	Lithuania
☐	AM	Armenia	☐	LU	Luxembourg
☐	AT	Austria	☐	LV	Latvia
☐	AU	Australia	☐	MD	Republic of Moldova
☐	AZ	Azerbaijan	☐	MG	Madagascar
☐	BA	Bosnia & Herzegovina	☐	MK	The former Yugoslav Republic of Macedonia
☐	BB	Barbados	☐	MN	Mongolia
☐	BG	Bulgaria	☐	MW	Malawi
☐	BR	Brazil	☐	MX	Mexico
☐	BY	Belarus	☐	NO	Norway
☐	CA	Canada	☐	NZ	New Zealand
☐	CH and LI	Switzerland and Liechtenstein	☐	PL	Poland
☐	CN	China	☐	PT	Portugal
☐	CU	Cuba	☐	RO	Romania
☐	CZ	Czech Republic	☐	RU	Russian Federation
☐	DE	Germany	☐	SD	Sudan
☐	DK	Denmark	☐	SE	Sweden
☐	EE	Estonia	☐	SG	Singapore
☐	ES	Spain	☐	SI	Slovenia
☐	FI	Finland	☐	SK	Slovakia
☐	GB	United Kingdom	☐	SL	Sierra Leone
☐	GD	Grenada	☐	TJ	Tajikistan
☐	GE	Georgia	☐	TM	Turkmenistan
☐	GH	Ghana	☐	TR	Turkey
☐	GM	Gambia	☐	TT	Trinidad and Tobago
☐	HR	Croatia	☐	UA	Ukraine
☐	HU	Hungary	☐	UG	Uganda
☐	ID	Indonesia	☒	US	United States of America
☐	IL	Israel	☐	UZ	Uzbekistan
☐	IN	India	☐	VN	Viet Nam
☐	IS	Iceland	☐	YU	Yugoslavia
☐	JP	Japan	☐	ZW	Zimbabwe
☐	KE	Kenya	☐		
☐	KG	Kyrgyzstan			
☐	KP	Democratic People's Republic of Korea			
☐	KR	Republic of Korea			
☐	KZ	Kazakhstan			
☐	LC	Saint Lucia			
☐	LK	Sri Lanka			
☐	LR	Liberia			
☐	LS	Lesotho			

Check-boxes reserved for designating States (for the purposes of a national patent) which have become party to the PCT after issuance of this sheet:

- ☐ AE United Arab Emirates
- ☐ Any other state which is party to the PCT
- ☐ .....

Precautionary Designation Statement: In addition to the designations made above, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except any designation(s) indicated in the Supplemental Box as being excluded from the scope of this statement. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation of a designation consists of the filing of a notice specifying that designation and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.)*

Supplemental Box *If the Supplemental Box is not used, this sheet need not be included in the request.*

Use this box in the following cases:

I. If, in any of the Boxes, the space is insufficient to furnish all the information:	*In such case, write "Continuation of Box No. ..." (indicate the number of the Box) and furnish the information in the same manner as required according to the captions of the Box in which the space was insufficient;*
in particular:	
(i) if more than two persons are involved as applicants and/or inventors and no "continuation sheet" is available:	*in such case, write "Continuation of Box III" and indicate for each additional person the same type of information as required in Box No. III. The country of the address indicated in this box is the applicant's state (that is, country) of residence if no state of residence is indicated below;*
(ii) if, in Box No. II or in any of the sub-boxes of Box No. III, the indication "the States indicated in the Supplemental Box" is checked:	*in such case write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the applicant(s) involved and next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is applicant;*
(iii) if, in Box No. II or in any of the sub-boxes of Box No. III, the inventor or the inventor/applicant is not inventor for the purposes of all designated States or for the purposes of the United States of America:	*in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the inventor(s) and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is inventor;*
(iv) if, in addition to the agent(s) indicated in Box No. IV, there are further agents:	*in such case, write "Continuation of Box No. IV" and indicate for each further agent the same type of information as required in Box No. IV;*
(v) if, in Box No. V, the name of any State (or OAPI) is accompanied by the indication "patent of addition," or "certificate of addition," or if, in Box No. V, the name of the United States of America is accompanied by an indication "Continuation" or "Continuation-in-part":	*in such case, write "Continuation of Box No. V" and the name of each State involved (or OAPI), and after the name of each such State (or OAPI), the number of the parent title or parent application and the date of grant of the parent title or filing of the parent application;*
(vi) if in Box No. VI there are more than three earlier applications whose priority is claimed:	*in such case, write "Continuation of Box No. VI" and indicate for each additional earlier application the same type of information as required in Box No. VI.*
(vii) if, in Box No. VI, the earlier application is an ARIPO application:	*in such case, write "Continuation of Box No. VI", specify the number of the item corresponding to that earlier application and indicate at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed.*
2. If, with regard to the precautionary designation statement contained in Box No. V, the applicant wishes to exclude any State(s) from the scope of that statement:	*in such case, write "Designation(s) excluded from precautionary designation statement" and indicate the name or two-letter code of each state so excluded.*
3. If the applicant claims, in respect of any designated Office, the benefits of provisions of the national law concerning non-prejudicial disclosures or exceptions to lack of novelty:	*in such case, write "Statement Concerning Non-Prejudicial Disclosures or Exceptions to Lack of Novelty" and furnish that statement below.*

Continuation of Box IV

ARMITAGE, IAN M.
BRASNETT, ADRIAN H.
BREWSTER, ANDREA R.
CALDERBANK, T. ROGER
CARTER, STEPHEN
COLEIRO, RAYMOND
CRIPPS, JOANNA E.
FORD, MICHAEL F.
GURA, H. ALAN
HACKNEY, NIGEL J.
HARRISON, DAVID C.
KIDDLE, SIMON J.
KREMER, SIMON M.
LINN, S. JONATHAN
LYONS, JUNE, M.
NICHOLLS, KATHRYN M.
O'BRIEN, CAROLINE J.
PAGET, HUGH C.E.
SANDERSON, MICHAEL J.
STONER, G. PATRICK
STUART, IAN
WALTON, SEÁN M.
WATKIN, TIMOTHY L.

Box No. I PRIORITY CLAIM ☐ Further priority claims are indicated in the Supplemental Box

Filing date of earlier application (day/month/year)	Number of earlier application	Where earlier application is: national application: country	regional application:* regional Office	international application: receiving Office
item (1) 1 MAY 1998	9809450.1	GB		
item (2)				
item (3)				

☒ The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) *(only if the earlier application was filed with the Office which for the purposes of the present international application is the receiving Office)* identified above as item(s): 1

* *Where the earlier application is an ARIPO application, it is mandatory to indicate in the supplemental box at least one country party to the Paris Convention fo the Protection of Industrial Property for which that earlier application was filed (Rule 4.10(b)(ii)). See Supplemental Box.*

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(If two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):*

ISA /

Request to use results of earlier search; reference to that search (if an earlier search has been carried out by or requested from the International Searching Authority):

Date *(day/month/year)* Number Country *(or regional Office)*

Box No. VIII CHECK LIST; LANGUAGE OF FILING

This international application contains the following number of sheets	
request	:4
description (excluding sequence listing part)	:37
claims	:6
abstract	:2
drawings	:8
sequence listing part of description	:0
Total number of sheets	:57

This international application is **accompanied by** the item(s) marked below:

1. ☒ fee calculation sheet
2. ☐ separate signed power of attorney
3. ☐ copy of general power of attorney; reference number, if any:
4. ☐ statement explaining lack of signature
5. ☒ priority document(s) *identified in Box No. VI as item(s)*:
6. ☐ translation of international application into (language):
7. ☐ separate indications concerning deposited microorganisms or other biological material
8. ☐ nucleotide and/or amino acid sequence listing in computer readable form
9. ☒ other *(specify)*:23/77

Figure of the drawings which should accompany the abstract 2

Language of filing of the international application: ENGLISH

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).

.....

CALDERBANK, T. ROGER
APPOINTED AGENT

For receiving Office use only

1. Date of actual receipt of the purported international application:	2. Drawings:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:	☐ received:
4. Date of timely receipt of the required corrections under PCT Article 11(2):	☐ not received:
5. International Searching Authority (if two or more are competent: ISA/	6. ☐ Transmittal of search copy delayed until search fee is paid

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

This sheet is not part of and does not count as a sheet of the international application.

PCT
FEE CALCULATION SHEET
Annex to the Request

For receiving Office use only

International application No.

Date stamp of the receiving Office

Applicant's or agent's file reference: TRC/BP5764824

Applicant: WANDEL & GOLDERMANN

CALCULATION OF PRESCRIBED FEES

1. TRANSMITTAL FEE..... £55 T

2. SEARCH FEE ..... £812 S

International search to be carried out by _____
(If two or more International Searching Authorities are competent in relation to the international application, indicate the name of the Authority which is chosen to carry out the international search.)

3. INTERNATIONAL FEE

Basic Fee

The international application contains 57 sheets.

first 30 sheets ..... £285 b_1

27 x £6 = £162 b_2
remaining sheets additional amount

Add amounts entered at b_1 and b_2 and enter total at B.... £447 B

Designation Fees

The international application contains 71 designations.

10 x £65 = £650 D
number of designation fees payable *(maximum 10)* amount of designation fee

Add amounts entered at B and D and enter total at I ..... £1097 I

(Applicants from certain States are entitled to a reduction of 75% of the international fee. Where the applicant is (or all applicants are) so entitled, the total to be entered at I is 25% of the sum of the amounts entered at B and D.)

4. FEE FOR PRIORITY DOCUMENT (if applicable) ..... £22 P

5. TOTAL FEES PAYABLE
Add amounts entered at T, S, I and P, and enter total in the TOTAL box

£1986
TOTAL

☐ The designation fees are not paid at this time.

MODE OF PAYMENT

- ☐ authorization to charge deposit account (see below)
- ☐ bank draft
- ☐ coupons
- ☒ cheque
- ☐ cash
- ☐ other *(specify)*
- ☐ postal money order
- ☐ revenue stamps

DEPOSIT ACCOUNT AUTHORIZATION *(this mode of payment may not be available at all receiving Offices)*

The RO/ ____ ☐ is hereby authorized to charge the total fee indicated above to my deposit account.

☐ is hereby authorized to charge any deficiency or credit any overpayment in the total fees indicated above to my deposit account.

☐ is hereby authorized to charge the fee for preparation and transmittal of the priority document to the International Bureau of WIPO to my deposit account.

Deposit Account Number _____ Day *(day/month/year)* _____ Signature _____

DESIGNATION OF STATES

Regional Patent

☐ **AP** **ARIPO Patent:** GH Ghana, GM Gambia, KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SZ Swaziland, UG Uganda, ZW Zimbabwe and any other State which is a Contracting State of the Harare Protocol and of the PCT

☐ **EA** **Eurasian Patent:** AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakstan, MD Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a member state of EAPC and a Contracting State of the PCT

☒ **EP** **European Patent:** AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, CY Cyprus, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT

☐ **OA** **OAPI Patent:** BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, GW Guinea-Bissau, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT

National Patent

☐ AE United Arab Emirates
☐ AL Albania
☐ AM Armenia
☐ AT Austria
☐ AU Australia
☐ AZ Azerbaijan
☐ BA Bosnia & Herzegovina
☐ BB Barbados
☐ BG Bulgaria
☐ BR Brazil
☐ BY Belarus
☐ CA Canada
☐ CH and LI Switzerland & Liechtenstein
☐ CN China
☐ CU Cuba
☐ CY Cyprus
☐ CZ Czech Republic
☐ DE Germany
☐ DK Denmark
☐ EE Estonia
☐ ES Spain
☐ FI Finland
☐ GB United Kingdom
☐ GD Grenada
☐ GE Georgia
☐ GH Ghana
☐ GM Gambia
☐ HR Croatia
☐ HU Hungary
☐ ID Indonesia
☐ IL Israel
☐ IN India
☐ IS Iceland
☐ JP Japan
☐ KE Kenya
☐ KG Kyrgyzstan
☐ KP Democratic People's Republic of Korea
☐ KR Republic of Korea
☐ KZ Kazakstan
☐ LC Saint Lucia
☐ LK Sri Lanka
☐ LR Liberia
☐ LS Lesotho
☐ LT Lithuania
☐ LU Luxembourg
☐ LV Latvia
☐ MD Republic of Moldova
☐ MG Madagascar
☐ MK Macedonia
☐ MN Mongolia
☐ MW Malawi
☐ MX Mexico
☐ NO Norway
☐ NZ New Zealand
☐ PL Poland
☐ PT Portugal
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☐ RU Russian Federation
☐ SD Sudan
☐ SE Sweden
☐ SG Singapore
☐ SI Slovenia
☐ SK Slovakia
☐ SL Sierra Leone
☐ TJ Tajikistan
☐ TM Turkmenistan
☐ TR Turkey
☐ TT Trinidad & Tobago
☐ UA Ukraine
☐ UG Uganda
☒ US United States of America
☐ UZ Uzbekistan
☐ VN Vietnam
☐ YU Yugoslavia
☐ ZW Zimbabwe

Check-boxes reserved for States which have become party to the PCT after issuance of this sheet

☐ ..... ☐ .....

Note: this sheet lists all States known to be PCT Contracting States at 10 March 1999

Mewburn Ellis, March 1999
3design.frm

WO 99/57842
PCT/GB99/01339

PATENT COOPERATION TREATY

09/674444

From the INTERNATIONAL BUREAU

PCT

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

To:
CALDERBANK, T., Roger
Mewburn Ellis
York House
23 Kingsway
London WC2B 6HP
ROYAUME-UNI

Date of mailing (day/month/year) 11 November 1999 (11.11.99)	
Applicant's or agent's file reference TRC/BP5764824	**IMPORTANT NOTICE**
International application No. PCT/GB99/01339	**International filing date** (day/month/year) 29 April 1999 (29.04.99)
Priority date (day/month/year) 01 May 1998 (01.05.98)	
Applicant WANDEL & GOLTERMANN et al	

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
   EP,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
   None

   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
   11 November 1999 (11.11.99) under No. WO 99/57842

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, **a demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer
J. Zahra

Telephone No. (41-22) 338.83.38

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING SUBMISSION OR TRANSMITTAL OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

CALDERBANK, T., Roger
Mewburn Ellis
York House
23 Kingsway
London WC2B 6HP
ROYAUME-UNI

RECORDS ENTD
RECORDS SENT
DIARY ENTD

Date of mailing (day/month/year) 23 June 1999 (23.06.99)	
Applicant's or agent's file reference TRC/BP5764824	**IMPORTANT NOTIFICATION**
International application No. PCT/GB99/01339	International filing date (day/month/year) 29 April 1999 (29.04.99)
International publication date (day/month/year) Not yet published	Priority date (day/month/year) 01 May 1998 (01.05.98)
Applicant WANDEL & GOLTERMANN et al	

1. The applicant is hereby notified of the date of receipt (except where the letters "NR" appear in the right-hand column) by the International Bureau of the priority document(s) relating to the earlier application(s) indicated below. Unless otherwise indicated by an asterisk appearing next to a date of receipt, or by the letters "NR", in the right-hand column, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).

2. This updates and replaces any previously issued notification concerning submission or transmittal of priority documents.

3. An asterisk(*) appearing next to a date of receipt, in the right-hand column, denotes a priority document submitted or transmitted to the International Bureau but not in compliance with Rule 17.1(a) or (b). In such a case, the attention of the applicant is directed to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

4. The letters "NR" appearing in the right-hand column denote a priority document which was not received by the International Bureau or which the applicant did not request the receiving Office to prepare and transmit to the International Bureau, as provided by Rule 17.1(a) or (b), respectively. In such a case, the attention of the applicant is directed to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

Priority date	Priority application No.	Country or regional Office or PCT receiving Office	Date of receipt of priority document
01 May 1998 (01.05.98)	9809450.1	GB	21 June 1999 (21.06.99)

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer

F. Gateau

Telephone No. (41-22) 338.83.38

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF RECEIPT OF RECORD COPY

(PCT Rule 24.2(a))

DESIGNATIONS AGREED WITH COMPUTER

To:

CALDERBANK, T., Roger
Mewburn Ellis
York House
23 Kingsway
London WC2B 6HP
ROYAUME-UNI

RECEIVED
14 JUN 1999

Date of mailing (day/month/year)	IMPORTANT NOTIFICATION
09 June 1999 (09.06.99)	
Applicant's or agent's file reference	**International application No.**
TRC/BP5764824	PCT/GB99/01339

The applicant is hereby notified that the International Bureau has received the record copy of the international application as detailed below.

Name(s) of the applicant(s) and State(s) for which they are applicants:

WANDEL & GOLDERMANN (for all designated States except US)
BREWER, Symon, Reuben (for US)

International filing date	:	29 April 1999 (29.04.99)
Priority date(s) claimed	:	01 May 1998 (01.05.98)
Date of receipt of the record copy by the International Bureau	:	25 May 1999 (25.05.99)
List of designated Offices	:	

EP :AT,BE,CH,CY,DE,DK,ES,FI,FR,GB,GR,IE,IT,LU,MC,NL,PT,SE
National :US

ATTENTION

The applicant should carefully check the data appearing in this Notification. In case of any discrepancy between these data and the indications in the international application, the applicant should immediately inform the International Bureau.

In addition, the applicant's attention is drawn to the information contained in the Annex, relating to:

- [X] time limits for entry into the national phase
- [X] confirmation of precautionary designations
- [X] requirements regarding priority documents

A copy of this Notification is being sent to the receiving Office and to the International Searching Authority.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer:

F. Gateau

Telephone No. (41-22) 338.83.96

ANNEX TO FORM PCT/IB/301

International application No.
PCT/GB99/01339

INFORMATION ON TIME LIMITS FOR ENTERING THE NATIONAL PHASE

The applicant is reminded that the "national phase" must be entered before each of the designated Offices indicated in the Notification of Receipt of Record Copy (Form PCT/IB/301) by paying national fees and furnishing translations, as prescribed by the applicable national laws.

The time limit for performing these procedural acts is **20 MONTHS** from the priority date or, for those designated States which the applicant elects in a demand for international preliminary examination or in a later election, **30 MONTHS** from the priority date, provided that the election is made before the expiration of 19 months from the priority date. Some designated (or elected) Offices have fixed time limits which expire even later than 20 or 30 months from the priority date. In other Offices an extension of time or grace period, in some cases upon payment of an additional fee, is available.

In addition to these procedural acts, the applicant may also have to comply with other special requirements applicable in certain Offices. **It is the applicant's responsibility** to ensure that the necessary steps to enter the national phase are taken in a timely fashion. Most designated Offices do not issue reminders to applicants in connection with the entry into the national phase.

For detailed information about the procedural acts to be performed to enter the national phase before each designated Office, the applicable time limits and possible extensions of time or grace periods, and any other requirements, see the relevant Chapters of Volume II of the PCT Applicant's Guide. Information about the requirements for filing a demand for international preliminary examination is set out in Chapter IX of Volume I of the PCT Applicant's Guide.

GR and ES became bound by PCT Chapter II on 7 September 1996 and 6 September 1997, respectively, and may, therefore, be elected in a demand or a later election filed on or after 7 September 1996 and 6 September 1997, respectively, regardless of the filing date of the international application. (See second paragraph above.)

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

CONFIRMATION OF PRECAUTIONARY DESIGNATIONS

This notification lists only specific designations made under Rule 4.9(a) in the request. It is important to check that these designations are correct. Errors in designations can be corrected where precautionary designations have been made under Rule 4.9(b). The applicant is hereby reminded that any precautionary designations may be confirmed according to Rule 4.9(c) before the expiration of 15 months from the priority date. If it is not confirmed, it will automatically be regarded as withdrawn by the applicant. There will be no reminder and no invitation. Confirmation of a designation consists of the filing of a notice specifying the designated State concerned (with an indication of the kind of protection or treatment desired) and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.

REQUIREMENTS REGARDING PRIORITY DOCUMENTS

For applicants who have not yet complied with the requirements regarding priority documents, the following is recalled.

Where the priority of an earlier national, regional or international application is claimed, the applicant must submit a copy of the said earlier application, certified by the authority with which it was filed ("the priority document") to the receiving Office (which will transmit it to the International Bureau) or directly to the International Bureau, before the expiration of 16 months from the priority date, provided that any such priority document may still be submitted to the International Bureau before that date of international publication of the international application, in which case that document will be considered to have been received by the International Bureau on the last day of the 16-month time limit (Rule 17.1(a)).

Where the priority document is issued by the receiving Office, the applicant may, instead of submitting the priority document, request the receiving Office to prepare and transmit the priority document to the International Bureau. Such request must be made before the expiration of the 16-month time limit and may be subjected by the receiving Office to the payment of a fee (Rule 17.1(b)).

If the priority document concerned is not submitted to the International Bureau or if the request to the receiving Office to prepare and transmit the priority document has not been made (and the corresponding fee, if any, paid) within the applicable time limit indicated under the preceding paragraphs, any designated State may disregard the priority claim, provided that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity to furnish the priority document within a time limit which is reasonable under the circumstances.

Where several priorities are claimed, the priority date to be considered for the purposes of computing the 16-month time limit is the filing date of the earliest application whose priority is claimed.

PATENT COOPERATION TREATY

From the **RECEIVING OFFICE**

PCT 09/674444

To:
Mewburn Ellis
York House
23 Kingsway
London

WC2B 6HP

NOTIFICATION OF THE INTERNATIONAL APPLICATION NUMBER AND OF THE INTERNATIONAL FILING DATE

(PCT Rule 20.5(c))

Date of mailing (day/month/year) 24/06/99

Applicant's or agents's file reference
TRC/BP5764824

IMPORTANT NOTIFICATION

International application No.	International filing date (day/month/year)	Priority date (day/month/year)
PCT/GB99/01339	29/04/1999	01/05/1998

Applicant
Wandel & Goltermann et al

Title of the invention
Jitter Measurement

1. The applicant is hereby notified that the international application has been accorded the international application number and the international filing date indicated above.

2. The applicant is further notified that the record copy of the international application:

☒ was transmitted to the International Bureau on 17/05/99

☐ has not yet been transmitted to the International Bureau for the reason indicated below and a copy of this notification has been sent to the International Bureau*:

☐ because the necessary national security clearance has not yet been obtained.

☐ because *(reason to be specified)*:

* The International Bureau monitors the transmittal of the record copy by the receiving Office and will notify the applicant (with Form PCT/IB/301) of its receipt. Should the record copy not have been received by the expiration of 14 months from the priority date, the International Bureau will notify the applicant (Rule 22.1(c)).

Name and mailing address of the receiving Office	Authorized officer
The Patent Office Cardiff Road, Newport South Wales NP9 1RH	G C Shadbolt GS
Facsimile No.	Telephone No. 01633 814586

Form PCT/RO/105 (July 1992)

The demand must be filed directly with the competent International Preliminary Examining Authority or, if two or more Authorities are competent, with the one chosen by the applicant. The full name or two-letter code of that Authority may be indicated by the applicant on the line below:

IPEA/_____

09/674444

PCT

CHAPTER II

DEMAND

under Article 31 of the Patent Cooperation Treaty:
The undersigned requests that the international application specified below be the subject of international preliminary examination according to the Patent Cooperation Treaty and hereby elect all eligible States (except where otherwise indicated).

For International Preliminary Examining Authority use only

Identification of IPEA	Date of receipt of DEMAND

Box No. I IDENTIFICATION OF THE INTERNATIONAL APPLICATION

Applicant's or agent's file reference: TRC/FP5764824

International application No.	International filing date *(day/month/year)*	(Earliest Priority date *(day/month/year)*
PCT/GB99/01339	29 APRIL 1999	1 MAY 1998

Title of invention: JITTER MEASUREMENT

Box No. II APPLICANT(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

WANDEL & GOLTERMANN
EUROTECH HOUSE
BURRINGTON WAY
PLYMOUTH
DEVON PL5 3LZ
GB

Telephone No.:

Facsimile No.:

Teleprinter No.:

State *(i.e. country)* of nationality: GB

State *(i.e. country)* of residence: GB

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

BREWER SYMON REUBEN
48 PEVERELL PARK ROAD
PEVERELL
PLYMOUTH
PL3 4NB
GB

State *(i.e. country)* of nationality: GB

State *(i.e. country)* of residence: GB

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

State *(i.e. country)* of nationality:

State *(i.e. country)* of residence:

☐ Further applicants are indicated on a continuation sheet.

International application No.
x

Box No. III AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The following person is [X] agent [ ] common representative

and [X] has been appointed earlier and represents the applicant(s) also for international preliminary examination.

[ ] is hereby appointed and any earlier appointment of (an) agent(s)/common representative is hereby revoked.

[ ] is hereby appointed, specifically for the procedure before the International Preliminary Examining Authority, in addition to the agent(s)/common representative appointed earlier.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

CALDERBANK, T.R.
Mewburn Ellis
York House
23 Kingsway
London WC2B 6HP
GB

Telephone No.: 020 7240 4405

Facsimile No.: 020 7240 9339

Teleprinter No.:

[ ] **Address for correspondence:** Mark this check-box where no agent or common representative is/has been appointed and th space above is used instead to indicate a special address to which correspondence should be sent.

Box No. IV BASIS FOR INTERNATIONAL PRELIMINARY EXAMINATION

Statement concerning amendments:*

1 The applicant wishes the international preliminary examination to start on the basis of:

[X] the international application as originally filed

the description
- [ ] as originally filed.
- [ ] as amended under Article 34

the claims
- [ ] as originally filed
- [ ] as amended under Article 19 (together with any accompanying statement)
- [ ] as amended under Article 34

the drawings
- [ ] as originally filed
- [ ] as amended under Article 34

2. [ ] The applicant wishes any amendment to the claims under Article 19 to be considered as reversed.

3. [ ] The applicant wishes the start of the international preliminary examination **to be postponed** until the expiration of 20 months from the priority date unless the International Preliminary Examination Authority receives a copy of any amendments made under Article 19 or a notice from the applicant that he does not wish to make such amendments (Rule 69.1(d)). *(This check-box may be marked only where the time limit under Article 19 has not yet expired.)*

* Where no check-box is marked, international preliminary examination will start on the basis of the international application as originally filed, or where a copy of amendments to the claims under Article 19 and/or amendments of the international application under Article 34 are received by the International Preliminary Examining Authority before it has begun to draw up a written opinion or the international preliminary examination, as so amended.

Language for the purposes of international preliminary examination: ENGLISH

- [X] which is the language in which the international application was filed.
- [ ] which is the language of a translation furnished for the purposes of international search.
- [ ] which is the language of publication of the international application.
- [ ] which is the language of the translation (to be) furnished for the purposes of international preliminary examination.

Box No. V ELECTION OF STATES

The applicant hereby elects all eligible States *(that is, all States which have been designated and which are bound by Chapter II of the PCT)*

excluding the following States which the applicant wishes not to elect:

International application No.
PCT/US99/06739

Box No. VI CHECK LIST

The demand is accompanied by the following elements, in the language referred to in Box No. IV, for the purposes of international preliminary examination			For International Preliminary Examining Authority use only: received	not received
1. translation of international application	: 0	sheets	☐	☐
2. amendments under Article 34	: 0	sheets	☐	☐
3. copy (or, where required, translation) of amendments under Article 19	: 0	sheets	☐	☐
4. copy (or, when required, translation) of	0	sheets	☐	☐
5. letter	: 1	sheets	☐	☐
6. other *(specify)*	: 0	sheets	☐	☐

The demand is also accompanied by the item(s) marked below:

1. ☐ fee calculation sheet
2. ☐ separate signed power of attorney
3. ☐ copy of general power of attorney; reference number, if any:
4. ☐ statement explaining lack of signature
5. ☐ nucleotide and or amino acid sequence listing in computer readable form
6. ☐ other *(specify)*:

Box No. VII SIGNATURE OF APPLICANT, AGENT OR COMMON REPRESENTATIVE

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the demand).

I.P. Calderbank I.A. STUART

APPOINTED AGENT

For International Preliminary Examining Authority use only

1. Date of actual receipt of DEMAND:
2. Adjusted date of receipt of demand due to CORRECTIONS under Rule 60.1(b):
3. ☐ The date of receipt of the demand is AFTER the expiration of 19 months from the priority date and item 4 or 5, below, does not apply. ☐ The applicant has been informed accordingly.
4. ☐ The date of receipt of the demand is WITHIN the period of 19 months from the priority date as extended by virtue of Rule 80.5
5. ☐ Although the date of receipt of the demand is after the expiration of 19 months from the priority date, the delay in arrival is EXCUSED pursuant to Rule 82.

For International Bureau use only

Demand received from IPEA on:

PATENT COOPERATION TREATY

09/674444

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

CALDERBANK, T., Roger
Mewburn Ellis
York House
23 Kingsway
London WC2B 6HP
GRANDE BRETAGNE

RECEIVED
28 JAN 2000

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT
(PCT Rule 71.1)

Date of mailing *(day/month/year)*	25.01.2000
Applicant's or agent's file reference TRC/EP5764824	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/01339	29/04/1999	01/05/1998

Applicant
WANDEL & GOLTERMANN et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Ahrens, R Tel.+49 89 2399-2668

Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
TRC/BP5764824		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/01339	29/04/1999	01/05/1998
International Patent Classification (IPC) or national classification and IPC		
H04L1/20		
Applicant		
WANDEL & GOLTERMANN et al.		

1. This International preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the International application

Date of submission of the demand	Date of completion of this report
30/11/1999	25.01.2000
Name and mailing address of the international preliminary examining authority:	Authorized officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Haas, H Telephone No. +49 89 2399 8800

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/01339

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-36 as originally filed

Claims, No.:

1-15 as originally filed

Drawings, sheets:

1/8-8/8 as originally filed

2. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/01339

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims 1-15
	No:	Claims
Inventive step (IS)	Yes:	Claims 1-15
	No:	Claims
Industrial applicability (IA)	Yes:	Claims 1-15
	No:	Claims

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

INTERNATIONAL PRELIMINARY EXAMINATION REPORT - SEPARATE SHEET

International application No. PCT/GB99/01339

SECTION V

The subject-matter of the international application relates to a method (claim 1) and an arrangement (claims 10 and 15) for measuring jitter in a digital signal.

The nearest state of the art is document D1 (US-A-4 975 634), where the jitter is determined by measuring the phase difference in terms of high speed clock counts between transitions of the jittered clock signal and a reference clock.

Furthermore D2 (EP-A-0 362 491) discloses a method of determining jitter where two voltages representing values of coarse and fine jitter measurements are summed for the final result.

To solve the problem of efficiently measuring jitter using only digital components, according to the main claims of the international application an offset reference clock is formed such that there are a predetermined number of sampling times in each bit. Jitter is measured by evaluating the occasions when the number of sampling times in a bit differs from the predetermined count.

This subject-matter is not rendered obvious, alone or in combination, by the documents of the International Search Report. Inventive activity and novelty are therefore acknowledged (Art. 33 (3) and (2) PCT).

The same applies to dependent claims 2 to 9 and 11 to 14.

As the subject-matter of the application relates to measurement devices, the criteria of industrial applicability is met (Art. 33 (4) PCT).

SECTION VII

Document D1 should have been briefly discussed in the description (Rule 5.1(a)(ii) PCT).

QL

2

REC'D 27 JAN 2000

WIPO PCT

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
TRC/BP5764824		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/01339	29/04/1999	01/05/1998
International Patent Classification (IPC) or national classification and IPC H04L1/20		
Applicant WAVETEC WADEL GOLTERMANN PLYMOUTH LIMITED		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/01339

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-36 as originally filed

Claims, No.:

1-15 as originally filed

Drawings, sheets:

1/8-8/8 as originally filed

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims 1-15
	No:	Claims
Inventive step (IS)	Yes:	Claims 1-15
	No:	Claims
Industrial applicability (IA)	Yes:	Claims 1-15
	No:	Claims

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

SECTION V

The subject-matter of the international application relates to a method (claim 1) and an arrangement (claims 10 and 15) for measuring jitter in a digital signal.

The nearest state of the art is document D1 (US-A-4 975 634), where the jitter is determined by measuring the phase difference in terms of high speed clock counts between transitions of the jittered clock signal and a reference clock.

Furthermore D2 (EP-A-0 362 491) discloses a method of determining jitter where two voltages representing values of coarse and fine jitter measurements are summed for the final result.

To solve the problem of efficiently measuring jitter using only digital components, according to the main claims of the international application an offset reference clock is formed such that there are a predetermined number of sampling times in each bit. Jitter is measured by evaluating the occasions when the number of sampling times in a bit differs from the predetermined count.

This subject-matter is not rendered obvious, alone or in combination, by the documents of the International Search Report. Inventive activity and novelty are therefore acknowledged (Art. 33 (3) and (2) PCT).

The same applies to dependent claims 2 to 9 and 11 to 14.

As the subject-matter of the application relates to measurement devices, the criteria of industrial applicability is met (Art. 33 (4) PCT).

SECTION VII

Document D1 should have been briefly discussed in the description (Rule 5.1(a)(ii) PCT).

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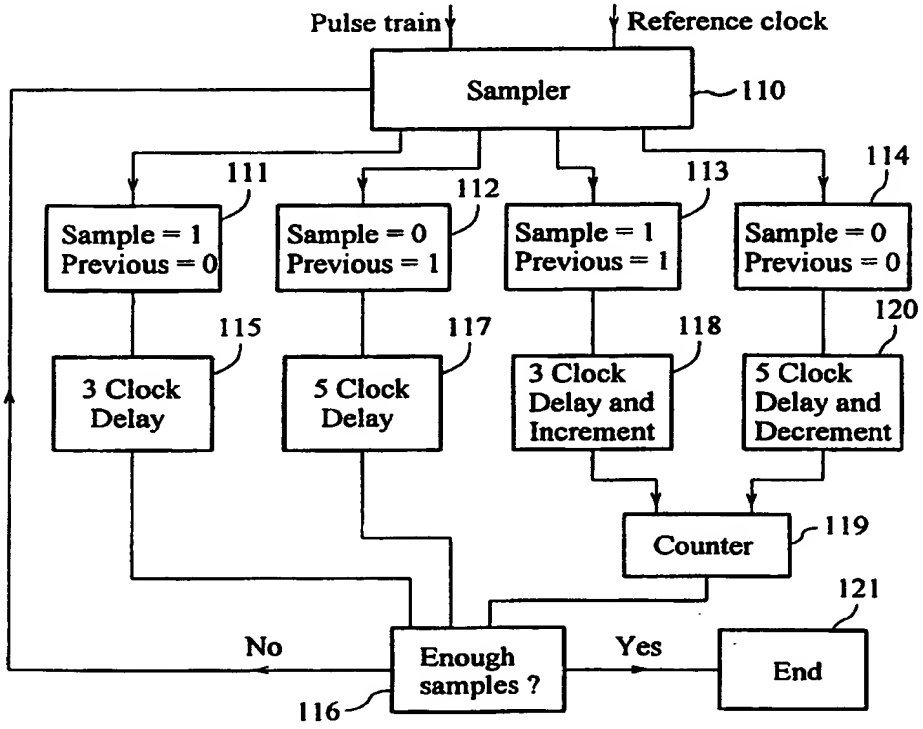
(54) Title: JITTER MEASUREMENT

(57) Abstract

The digital signal is sampled (110) at sampling time derived from an offset reference clock signal (101, 102, 103) so that, in the absence of jitter and said offset by a predetermined frequency, there are a predetermined number of sampling times in each bit of said digital signal. Once the samples of the digital signal have been obtained, a count (119) is made of the occasions when there are more or less than the predetermined number of sampling times within any bit of the digital signal over a predetermined period, counting up when the occasion is greater than the predetermined number and down when the occasion is less than the predetermined number. A coarse jitter measurement is then obtained by determining the differences between the maximum count value and the minimum count value minus and divided by an integer value. In addition, a fine jitter measurement is obtained.



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JITTER MEASUREMENT

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to the measurement of jitter in a digital signal. In theory, the spacing of the transitions between levels of a digital signal have a completely uniform spacing. In practice, particularly during transmission, there may be minute variations in the actual time of the transition, relative to the theoretical transition time defined by an absolute reference clock. These variations are referred to as jitter, and may be considered to be a spurious phase modulation of the signal.

SUMMARY OF THE PRIOR ART

Known systems for measuring jitter involve a very stable phase-locked loop which compares the pulse train containing jitter with an internally generated, jitter-free reference clock. The phase-locked loop has a generator for generating the reference clock, the output of which is fed to the input of a phase demodulator which also receives a digital signal containing jitter. The phase demodulator converts the signal to pulse duration modulation, which is output to a low pass filter, the output of which gives the jitter measurement, and also is fed back to the input of the reference clock generator, to form the loop. The low pass filter has cut off

frequency of 5-10% of the bit rate. But since the digital signal being investigated may contain long sequences of digital zeros, a pattern/clock converter may be used to convert the digital signal into a continuous pulse train with the same jitter as the original signal, which pulse train then forms the input to the phase demodulator. Analysis of the output may involve peak value rectification before the results are displayed, and/or analysis with a spectrum analyser.

As mentioned above, such a jitter measurement system involves a low pass filter, and this has a significant influence on the greatest measurable jitter frequency component. The known systems also involve many analog circuits, which are more expensive than digital components.

SUMMARY OF THE INVENTION

Therefore, the present invention seeks to provide a system for measuring jitter in a digital signal, in which a clock signal is extracted from the original digital signal, offset by a predetermined frequency, and smoothed to eliminate jitter therefrom. This gives an offset reference clock signal which is then used to sample the original input signal. Preferably, that offset clock signal is frequency multiplied by an integer factor before it is used for timing the sampling.

The effect of the offset of the reference clock

signal is that the sampling point is not fixed relative to the transition point over the bits of the input signal, but instead moves relative thereto. The sampling points are then arranged such that, in the absence of the offset and in the absence of jitter, there is a predetermined number of sampling points (normally only one, but this is not essential) in each successive bit. The present invention then proposes that the occasions when a bit of said digital signal contains other than the predetermined number of sampling points are detected. The occasions when the number of sampling points differs from the predetermined number occur because of the offset of the clock, but also due to jitter when the sampling point approaches the theoretical (absolute) transition point of the bits, being the transition point that would occur in the absence of jitter. The count of the number of occasions a bit has more sampling points than the predetermined number for a suitable measuring duration then gives a measure of the jitter.

Note that a bit may have more samplings than the predetermined number and a later bit may have fewer samplings than the predetermined number and both are occasions to be counted. For simplicity, the number of samplings per bit in the absence of offset and jitter is preferably one. Then, a count is made of the occasions there are either two sampling times within a bit on no

sampling times within a bit. It would also be possible to have more than one sampling time within a bit in the absence of offset and jitter, e.g. 2. Then the number of occasions of 3 or 1 sampling times in a bit would be counted.

The measurement period is preferably inversely proportional to the product of the bit rate and the difference between the original frequency and the offset frequency. Where the offset frequency is multiplied by an integer, the measurement period may be divided by that integer.

It is possible for the sampling to be at fixed intervals. However, where the offset clock signal is frequency multiplied by an integer factor, it is preferable that the sampling points are not regularly spaced by that integer factor, but are spaced by factors greater than or less than the integer factor. For example, if the integer is 4, then sampling may be at 3 and 5 intervals of the multiplied offset clock signal.

Thus a count is made of the occasions when there are more or less samplings, within the same bit than the predetermined number and the results of that count may be stored in a table whose size corresponds to the number of samples. The value stored in the table may increment and decrement depending whether the count is above or below the predetermined number. The value stored in the count

thus increments and decrements depending on the jitter, with the increments and decrements occurring as the sampling point is close to the absolute transition point of the bits. It is then possible to use the difference between the maximum value counted and the minimum value counted, possibly with 1 subtracted, to be multiplied by the bit period to derived a coarse jitter value. Moreover, if the number of samples between the first occurrence of the maximum value and the last of the occurrence of the minimum value is determined, divided by the total number of samples, a fine jitter value may be determined. The jitter amplitude is then given by the sums of these two values.

It should be noted that where the offset clock is multiplied by an integer value, both of these values may need to be divided by that integer to obtain a jitter value which corresponds to the peak-to-peak value of the deviation of the phase function of the measured signal relative to time. It can also be noted that such a measurement is independent of bit rate, and independent of the shape of the binary signals being measured.

Thus, an aspect of the present invention may provide a system for measuring jitter in a digital signal having means for deriving a first clock signal from the digital signal, the first clock signal being offset by a predetermined frequency from the digital signal and being

smoothed, means for sampling the digital signal using the first clock signal, such that, in the absence of jitter and said offset by a predetermined frequency, there are a predetermined number of sampling times in each bit of said digital signal, means for detecting occasions when the number of sampling times in any bit is different from the predetermined number, means for counting such occasions, and means for deriving a measurement of jitter from that count.

Another aspect of the invention relates to a method of measuring jitter using such a system.

The present invention, because it involves digital sampling and counting, can be embodied in a device which makes less use of analog circuits than known jitter measurement systems, which makes embodiments of the invention easier to produce.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 shows a schematic block diagram of a jitter measurement device being an embodiment of the present invention;

Fig. 2 is a flow-chart of the sampling sequence in the embodiment of Fig. 1;

Fig. 3 is a block diagram of components of the

jitter measurement device of Fig. 1;

Fig. 4 shows in more detail a part (RXBERT) of the diagram of Fig. 4;

Fig. 5 shows in more detail another part (RXJITTER) of the block diagram of Fig. 3;

Fig. 6 shows in more detail yet another part (TXBERT) of the block diagram of Fig. 3 and

Fig. 7 shows in more detail yet another part (TXJITTER) of the block diagram of Fig. 3.

DETAILED DESCRIPTION

Fig.1 shows schematically a jitter measurement device according to an embodiment of the present invention. In Fig.1, a digital pulse train signal which may contain jitter is fed to an input 100, and passed to a pattern clock converter 101. The converter 101 performs a similar function to that in the known systems, in that it converts the digital pulse train received at input 100, which may contain gaps in its pulse-train, into a continuous pulse-train with the same jitter as the original signal. That continuing pulse-train is then passed from the converter 101 to a clock frequency offset circuit 102. The offset circuit 102 determines the frequency of the pulse-train received from the converter 101 using known clock recovery techniques, but then is offset by a frequency which is a small proportion of the frequency of the pulses received.

The offset clock pulses thus generated are passed to a phase locked loop (PLL) 103 with a long time constant. The loop has a phase comparator, a low pass filter and a voltage controlled oscillator, with the low pass filter having a very low cut off frequency it thus separates the relatively weak jitter component from the stronger modulation which is symmetric about the working frequency of the phase comparator. Therefore a slow- acting control voltage is produced which is used to regulate the oscillator to produce an average, constant phase. This generates a jitter-free pulse-train which can thus be used for a reference clock.

In this embodiment, the pulse-train thus generated is frequency multiplied by an integral factor. In the subsequent description, it will be assumed that integer factor is 4, but the embodiment is not limited to this. Thus, the output of the PLL 103 is a reference clock with a frequency multiplied by 4, and offset from the frequency of the digital signal received at the input 100 by a small frequency.

That reference clock is passed to a data sampler 104, and is used to sample the pulse-train received at the input 100. As can be seen from Fig.1, the pulse-train input at input 100 is passed to the data sampler 104, as well as to the convertor 101. The action of that data sampler 104 will now be described with reference to

the flow chart of Fig.2.

As can be seen in Fig.2 a sampling step 110 is carried out, in which the pulse-train received at input 100 is sampled at a time determined by the reference clock signal from PLL 103. The logical level of the sample is then compared with that of the previous sample. There are four possibilities. In two of them, shown at steps 111 and 112, the sample is different from the previous sample, being either a change from logical zero to logical one (step 111) or a change from logical one to logical zero (step 112). In the other two alternatives, the sample is the same as the previous sample. In step 113, both are at logical one, and in step 114 both are at logical zero. From step 111, a three clock delay is imposed at step 115 and, assuming that the sampling operation has not yet been completed (step 116), processing returns to sampling step 110 for another sample. A similar procedure occurs at step 112, except that a five clock delay is imposed at step 117.

If there was no offsetting of the reference clock from the PLL 103, and the pulse-train received at input 100 had no jitter, then the effects of steps 111, 112, 115 and 117 would be for the sampling to switch across the logical transition of the pulse-train. If the sample was at logical level one, but had previously been a logical level zero, corresponding to step 111, the three

clock delay would move the sampling point back to logical level zero. Similarly, if the sampling was at logical level zero and the previous sampling at logical level one, the five clock delay 117 would move the sampling point back to logical level one. Thus, without offset and without jitter, the processing would pass alternately via steps 111 and 112.

However, the offset circuit 102 output pulses to the PLL 103 which have an offset frequency relative to the pulse train received at input 100. Thus, and still assuming that there is no jitter in the pulse-train received at input 100, a sampling point which is initially spaced from the transition between logical levels would slowly move towards that transition, and would eventually reach it. As it crossed the transition, two sampling points would occur within the same pulse, and thus the step 113 would be triggered. From step 113, a three clock delay again occurs at step 118, but also a signal is passed to a counter step 119 which increments a counter (not shown in Fig. 2) by one. From counter step 119, processing again passes to the sampling step 110 via step 116. After the sampling point had crossed the transition, it would again return to the options envisaged by steps 111 and 112, the counter step 119 would not again be triggered.

Thus, in the absence of jitter and over a sampling

period equal to the inverse of four times the clock offset times the reference clock, counter step 119 would be triggered only once. It can be observed from Fig. 2 that if the movement of the sampling point was within a logical zero, indicated by step 114, a five clock delaying step 120 would be triggered, and the counter step 119 activated to decrement the counter. Thus, in this case, the counter would count down once.

Now consider the effect of jitter in the pulse-train received by sample 100. In the subsequent discussion, the position of the transitions in the pulse-train in the absence of jitter will be called the absolute transition point, to distinguish from the actual transition point. These two transition points differ due to jitter. Whilst the sampling point is remote from the absolute transition point, the processing envisaged by Fig.2 will pass alternately via steps 111 and 112, assuming that the magnitude of jitter is less than the pulse width of the output of the PLL 103. However, as the sampling point approaches the absolute transition point, due to the offset of the reference clock, there is a possibility that a sampling point will occur within the same pulse as the previous sampling point, due to jitter. At that time, either step 113 or step 114 is triggered, and the counter step 119 either increments or decrements the counter.

Thus, over a part of the total sampling period, the counter step 119 may be triggered several times, depending on the magnitude of the jitter. It is this variation in the counter triggered by counting step 119 which enables jitter to be measured, as will now be described. Due to the jitter, the values stored by the counter triggered by counter step 119 will count up and down as steps 113 and 114 are triggered, if it is possible that the steps 113 and 114 may not be triggered alternately so that the counter step 119 may be triggered by the increment of step 118 more than once, before the counter step 119 is triggered by decrement step 120. It is also possible, of course, for the decrements at step 120 to be triggered more than once. As a result, over a measurement cycle, the counter may count up to a maximum value, and down to a minimum value. This is then used to determine the jitter as will now be described.

Referring again to Fig.1, the counter step 119 triggers an accumulator 105, which detects the counts and passes them to a store 106 to be stored in a table of a size corresponding to the measurement period. At the end of measurement period, triggered by end step 121, the difference between the maximum counts stored and the minimum counts stored, is determined. If there were no jitter, the minimum count would be zero (or minus one) and the maximum count would be one (or zero). If there

is jitter, however, either the maximum count or the minimum count may differ from that. Therefore, 1 is subtraced from the difference between the maximum count and the minimum count and multiplied by a quarter of the bit period of the input pulse-train received at input 100. This one quarter multiple occurs because of the multiplication of the reference clock. This measurement gives a value known as "coarse jitter". Secondly, the count table accumulator 105 is scanned to find the first occurrence at the maximum value count, and the last occurrence at the minimum value count. The difference in position is determined, divided by four and divided by the table size, which is equalled with a number of times the sampler 110 will be triggered during a measurement cycle. This gives a value known as the fine jitter. The sum of the course and fine jitter measurements are the peak-to-peak amplitude of the phase jitter of the input signals.

It can be noted that the term "jitter amplitude" designates the peak-to-peak value of the deviation of the phase function relative to time. The jitter amplitude is measured relative to the length of a clock period, so that it is independent of the shape of the binary signal of the pulse-train. Also, it is independent of bit rate, because it is relative to the clock period, making it a normalised parameter. It is thus possible to use this

value to compare jitter amplitudes.

Moreover, and as shown in Fig.1, the output of the table of store 106 may be passed to additional filter 107, or a discrete Fourier transform carried out on the count values stored. This enables the frequency content of the phase jitter of the input pulse-train received at input 100 to be determined.

In the embodiment described above, the PLL 103 multiplies the offset clock frequency generated by offset circuit 102 by 4. Other factors are useful, but it should be noted that this factor then determines the delays in steps 115, 117, 118 and 120 in Fig.2, and also the period of time of the measurement before end step 121 is reached. If, for example, a multiplier of 8 was used then steps 115 and 118 may have a seven clock delay, and steps 117 and 120 may have a nine clock delay. Moreover, the measurement period is then equal to the inverse of eight times the bit rate times the clock offset. Finally, when the fine jitter is measured, the subtraction of the table position of the first maximum value count from the table position of the last minimum count would then be divided by eight.

Fig. 3 is the top level functional block diagram for the entire jitter measurement device. It contains five main sections of circuitry, RX bit error rate testing (RX BERT) 10, TX bit error rate testing (TX BERT)

11, RX jitter 12, TX jitter 13 and V40 interfacing circuitry 14. The configuration can generate transmit jitter and also measure the incoming receive jitter while carrying out a bit error rate test at the same time. The V40 circuitry 14 controls operation of the configuration via V40 interface circuitry.

In the device of Fig. 3, the signals considered are shown in Table 1.

Table 1

Signal Name	Description
AD(0:7)	This signal is the V40's databus and the lower 8 bits of its address bus multiplexed together. Data travels backwards and forwards along this bus between the configuration and the V40.
AI(8:15)	This is the top 8 bits of the V40's address bus. It is an input to the configuration and indicates which address the V40 is accessing.

ASTB	This is the address/signal from the V40. It is high when the V40 is presenting its address on its external bus.
BEEPER	This signal oscillates at 2 megacycles per second and is divided in the smaller xilinx to form the beep signal.
CLKIN	This signal comes from the oscillator on the PAX A board and oscillates at 12.288 megahertz.
CLKOUT	This signal is derived from signal CLKIN and oscillates at twice the frequency of CLKIN ie at 24.576 megahertz.
COMP	This is the comparison output to the phase lock loop. It is used in the generation of the received jitter clock SCLK.
COUNT	This signal indicates when a received jitter phase change is to be counted. It is high for phase changes of both plus a quarter of an interval and minus a quarter of an interval. The direction of the COUNT is controlled by the signal UP.
CRCERR	This signal pulses whenever received CRC error happens.
D(0:7)	This is the internal databus to the configuration. It carries all the data from the V40 to and from the configuration.

	It also carries the data which is stored in the V40's memory during DMA accesses.
DLTCLK	This signal oscillates at the same period as the transmit clock. It is fed to the Dallas chip to provide the transmit clock. It is also used to ensure the signals XTPOS and XTNEG have the right mark space ratio.
DMAACK	This signal comes from the V40 and indicates that a DMA cycle is occurring.
DMARQ	This signal is generated by the configuration and is used to indicate to the V40 that a DMA request is pending.
DOJIT	This signal goes high whenever a twelfth of a unit interval jitter hit is to be inserted into the transmit jitter. The transmit jitter is comprised of a twelfth of a unit interval hits.
E1CLK	This signal goes high once per received bit

	in the RX jitter circuitry. Pulses on the E1CLK are counted and after every 8 counts a jitter result is DMA'd into the V40's memory.
FASERR	This signal pulses whenever the receiver detects a FAS error.
HLDRQ	This signal is passed to the V40 and is held permanently low in this configuration.
INJERR	The V40 controls the signal and can pulse it in order to inject a bit error into the transmit Bert pattern.
IOEN	This signal is used whenever the V40 carries out a IO operation.
IORD	This signal goes low whenever the V40 is carrying out a IO read instruction.
IOWR	This signal goes low whenever the V40 carries out an IO rate instruction.
JCLKI	This signal is sourced from the jitter attenuator chip. It oscillates at the same frequency as the receive clock less $1/(3 \times 2^{18})$ (approximately 1.27 parts per million). This signal is quadruple in frequency to form signal SCLK which is used to sample the received jitter.
JITAMP	This signal goes high whenever the V40 is writing to the jitter amplitude register on the transmit jitter circuitry.

JMODI	The transmit jitter waveform. It indicates whether the jitter waveform is varying in phase or otherwise.
JQ(0:2)	These signals are high whenever the V40 is writing to the transmit jitter frequency registers.
MNADDR	This signal is high wherever the received jitter circuitry has taken a jitter sample which is less than or equal to the previous minimum jitter sample. It causes the configuration to latch the DMA address of the next DMA cycle. At the end of the received jitter measurement the V40 reads this address to determine the received jitter.
MRD	This signal goes low whenever the V40 executes a memory read instruction.
MWRD	This signal goes low whenever the V40 executes a memory write instruction.
MWRI	This signal goes low whenever the V40 executes a memory write instruction.
MXADDR	This signal goes high whenever the received jitter measurements is higher than any of the previous received jitter measurements. This signal is used to latch an address which is later used by the V40 to determine

	the received jitter.
OFFCLK	This signal is the received clock offset by $-1/(3 \times 2^{18})$ (approximately -1.27 parts per million). This signal has quarter of a unit interval hits on it and is dejittered using the jitter attenuator chip.
RSERI	This is similar to RSER.
RSTS	This signal from the Dallas chip goes high during time slot 16 of the E1 frame and is decoded to indicate phase or CRC errors.
RXCKEN	This is the received clock enable signal for the RX Bert circuitry. It goes high for one CLKOUT period each received bit.
RXER	This signal is the data signal to the WG gate array.
RFER	This signal from the Dallas chip is de-coded to indicate FAS or CRC errors.
RFSYNC	This signal is used to synchronise the received time slot selection circuitry and also de-coded to indicate phase or CRC errors.
RSER	This is the E1 data from the Dallas chip. It is passed to the WG gate ray to measure bit errors.
RSTS	This signal from the Dallas chip goes high during time slot 16 of the E1 frame and is

RECONEN	This signal is used to reconfigure the xilinx when the jitter test is complete.
RCHCLK	This signal from the Dallas chip is the channel clock for the E1 receive frame. It is de-coded to indicate FAS or CRC errors.
RDLCLK	This is the receive clock which is passed to the Dallas chip. It is similar to signal RXCKEN but is extended by one clock period to meet the Dallas chip specifications.
SCLK	This is the master clock used by the RX jitter circuitry. It oscillates at normally 8.192 megahertz, minus $1/(3 \times 2^{18})$ (approximately 1.27 parts per million). It is used to sample in incoming received data to detect jitter.
SIGIN	This is the signal input to the 4046 phase up loop. It is used to quadruple the signal JCLKI to form signal SCLK.
SMP(0:7)	This signal is the raw sample jitter from the received jitter circuitry.
STOPPED	This signal is controlled by the V40 and is driven high when the received jitter measurement is stopped.
PDLCLK	This signal is the 2 megabit transmit clock generated from the transmit BERT circuitry.

	transmit jitter circuitry to insert a 12th of a unit interval jitter hit into the transmit clock. This signal prevents jitter hits from being inserted while the transmit bit is marking. This makes sure that the transmitted bits meet the pulse mask.
TMO	This signal originates in the Dallas chip and indicates the start of the transmit multiframe. It is used to synchronise the transmit time slot select circuitry.
TNEG	This signal originates in the Dallas chip and together with signal TPOS forms the transmit E1 stream.
TPOS	This signal originates in the Dallas chip and is used to generate the E1 stream.
TWO	This signal goes high when ever the received jitter is too much for the received jitter circuitry to cope with. The V40 can read whether this line as ever been high. If this is the case then the jitter measurement is discarded.
TXBERT	This signal goes high during time slots where bit error rate test signals are being transmitted.
TXBRTS	This signal goes high whenever a transmitted PRBS bit is to be sent.

TXCKEN	This signal goes high for one CLKOUT period each transmit bit.
TXCLK	This is the signal pass to the counter timer chip to indicate the transmit bit rate.
TSPDAT	This is the transmitted PRBS signal which is injected into the transmit data stream.
UP	This signal indicates the polarity of a receive jitter phase change and is used in conjunction with signal COUNT to accumulate the received jitter.
V24RX	This signal is the received V24 data which is passed to the V40.
V24RXD	This signal is the same as signal V24RX.
V24TX	This is the V24 data from the V40 transmitted out of the V24 port.
V24TXD	This signal is the same as V24TX.
VCO	This signal comes from the 4046 phase lock loop. It is used in the process whereby signal JCLKI is quadruple in frequency to form signal SCLK.
WGCLK	This signal is used to clock data into the WG gate array during bit error tests. The WG gate array then measures bit errors.
WGDATA	This is the data passed to the WG gate array from the receive BERT circuitry. It

	is used to perform bit error rate tests on.
WGERR	This signal originates in the WG gate array and indicates when a received bit error has occurred. It is passed to a counter timer chip where bit errors are measured.
XRNEG	This is the re-timed received E1 data which is passed to the Dallas chip.
XRNEGI	This is the raw E1 data from the B board.
XRBLS	This is the re-timed received E1 data which is passed to the Dallas chip.
XRPOSI	This signal is the raw received E1 data from the B board.
XSM	This signal is XRNEGI re-timed to the clock CLKOUT. The received clock is recovered from this signal.
XSP	This is the signal XRPOSI re-timed to the clock CLKOUT. Along with signal XSM this signal is used to generate the received clock.
XSPU	This is the unbuffered received E1 data which is passed to the jitter detection circuitry. Jitter is detected on this signal.
XTNEG	This signal is passed to the B board and is used to generate the transmit E1 string.
XTPOS	This signal is passed to the B board and is

	used to generate the transmit E1 string.

The various components of the system of Fig. 3 will now be considered in more detail. Starting with the RX bit error rate testing circuitry (RX BERT) 10, the detailed structure of this circuitry is shown in more detail in Fig. 4. As can be seen, there are several circuit elements. The first is CLOCK GEN component 20 is used to double the frequency of the signal CLKIN. This forms a higher frequency clock CLKOUT which has a frequency of about $25^{1}/_{2}$ meahertz. The logic for this clock doubling is placed in a CLB map at position AA. This ensures that the logic is very close on the LCA to the global clock buffer GCLK. The circuit works by forming a signal CLKBUF which is identical to the signal CLKIN except delayed by a small amount of time. The clock CLKOUT is passed to a GETCLOCK component 21.

This GETCLOCK component 21 recovers the clock from the received E1 data to be used in the TX Bert circuitry. The raw incoming E1 data is sampled by the system clock CLKOUT and then the positive and negative streams are gated together to form signal RESET. This signal resets a four bit divided by twelve counter. This counter is then used to generate received blocks during times when there are no marks on the received data. CLB map in this

drawing is used to try and squash as much logic as possible into the system. Thus, the GETCLOCK component 21 corresponds to the pattern clock converter 101 in Fig. 1.

The signals shown in Fig. 4 are then listed in Table 2.

Table 2

Signal Name	Description
CLKOUT	This is the 24½ megahertz system clock.
CNT0 through to CNT3	These four signals form a divide by twelve counter. It is divide by twelve as the received bit rate is a twelfth of the system clock. This counter is reset by the signal RESET. This occurs whenever a mark is received on the incoming data.

	During strings of 0's where there is no timing information on the received E1 data then this counter is used to 1 generate the signal RXCKEN which is the received clock enable.
RDLCLK	This signal is generated for the Dallas chip. The signal RXCKEN is only one CLKOUT clock period wide. This is not a wide enough pulse to clock the Dallas chip so the extra signal RDLCLK is generated which is twice as long to clock the Dallas chip.
RESET	This signal pulse is high whenever a mark is received on the incoming E1 data and is used to synchronise the received counter.

RNEG	This signal is fed to the Dallas chip and is the received negative E1 data.
RNEG0	This is the same signal as RNEG.
RPOS	This is the received E1 positive pulses which are fed to the Dallas chip.
RPOS0	This is the same signal as RPOS.
RXCKEN	This signal is generated in his block and is the received clock enable. This signal goes high for one CLKOUT period every single received bit.
RXP	This signal is used in combination with signal RXCKEN to generate the signal RDLCLK which is used to clock the Dallas chip.

The component 22 is used to generate the enables for the RX BERT circuitry. A patched signal USERTA goes high whenever the received data is to be passed to the WG gate array for PRBS testing. Two other CLB maps are used simply to compress the logic into the smallest space as possible. The block consists of an 8 bit

counter which is formed by signals CNT0 through to CNT7. This counter is reset to 0 by the signal RFSYNC from a Dallas chip 23. This counter is then de-coded to form the time slot select for the received PRBS data. Note that the high ordered 5 bits of the counter from signal CNT3 through to CNT7 are reset by the signal RFSYD. Again this technique is used to try and conserve space. The signal USERTS which is patched is then gated with the received clock enable to form the clock to the WG gate array which is signal WGCLK.

As mentioned above, the TSSEL component 22 receives the signal RFSYNC from the Dallas ship 23. That signal is then passed to a G703ERRS component 24. This component 24 is used to generate the CRC and FAS error signals. These signals are generated from gated signals from the Dallas chip 23. The signal CRC error goes low whenever the signals RF since and RFER are high simultaneously, likewise the signal FASERR goes low whenever the signals RCHCLK and RFER are high while the signal RSTS is low.

Next the RX jitter circuit 12 will be considered in more detail. Its internal structure is shown in Fig. 5. Again, it has several circuit elements. The first is a CLOCKOFF component 30. The component 30 offsets the incoming received E1 clock by minus $1/(3 \times 2^{18})$ (approximately 1.27 parts per million) before passing

this clock to a Dallas jitter attenuator 31. It has a function which is used to divide the receive clock by 65,536. It also contains test functions and SLPYREG which are used to offset the clock by adding single periods of the clock CLKOUT every 65,536 received bits. Thus, the CLOCKOFF component 30 corresponds to the offset circuit 102 in Fig. 1.

The CLIPYCNT function uses a four bit counter which performs a divide by twelve operation. Bits zero and one divide by three, and bits two and three divide by four, given a total of divide by twelve. The counter clock enabled by signal SLIPEN which goes high for one CLKOUT clock period every 65,536 received bits. The output of the counter is used to determine where in the twelve bit shift register in function SLIPYREG the received clock is inserted. In this way twelfth of a unit interval phase changes are introduced into the received clock in order to offset it by minus 1.27 parts per million. The SLIPYREG function uses a twelve bit shift register. It is used to inject slowly increasing twelfth of a unit interval jitter phase hits into received clock. Every 65,536 the point at which the received clock is injected into the shift register is moved closer to the beginning of the shift register. The output of the shift register ie the offset clock is at the last twelfth tap. When finally the RX clock has

been injected into the first bit of the shift register and it is time to access another twelfth of a unit interval phase shift. This received clock is discarded and then the received clock is then injected into the end of the shift register. In this way the clock is offset. The MISSCNT function uses a linear feedback shift register counter. It consists of a sixteen bit shift register, of which four taps are fed back to the input. Other gates are used to detect when the shift register counter has reached its terminal count. This forms signal HIGHNR which is the output .

Fig. 5 shows that the output JCLKI of the Dallas jitter attenuator 31 passes to a PLLSTUFF component 32. This PLLSTUFF component 32 is used to multiply the signal JCLKI by four to form the jitter sample block SCLK. It does this by doubling the frequency using the phase lock loop and then doubling the frequency from the phase up loop by two using an edge detection method. The Dallas jitter attenuator jitter 31 acts a phase lock loop which acts to remove the jitter component from the OFFCLK signal derived from the CLKOFF component 30. This function of the Dallas jitter attenuator 31, together with the PLLSTUFF component 32 thus form the PLL 103 of Fig. 1 which, as previously described, produces a jitter-free pulse-train, and then multiplies that pulse-train by the integer factor of 4.

A JITDET component 33 samples the incoming E1 data and from this measures the received jitter. It also recovers an E1 receive clock from the incoming E1 data stream. Thus, the JITDET component 33 forms the data sampler 104 in Fig. 1. It receives the offset and multiplied clock signal from PLLSTUFF component 32, and also the incoming signal which is being sampled for jitter.

A JITCOUNT component 34 generates the 8 bit jitter sample data. It consists of an 8 bit up/down counter which is enabled by the signal COUNT and the direct of the count is controlled by signal UP. The counter is set to value 80 HEX while the signal STOPPED is high. Notice that signal CNT7 is inverted before emerging from this component 34. Thus the JITCOUNT component 34 forms the accumulator 105.

The output from this JICOUNT component 34 is signal SMP(0:7). That output SMP(0:7) passes to a JITOUT component 35. This component 35 is used to transfer measured jitter into the V40's memory. This memory forms the sampler 106 of Fig. 1. It is also used to detect the amplitude of the received jitter. It does this by storing the addresses of the first time that a maximum valued jitter sample was stored and also the address of where the last minimum value jitter sample was stored. The difference between these addresses

ratio to the size of the whole DMA buffer gives an indication of the jitter amplitude. The current value of the sample jitter is stored in a shift register, along with the maximum value recorded up until now and the minimum value recorded up until now. These are compared in a block called compare which indicates when bigger or smaller samples are received. These signals are processed to generate latches for addresses.

Next the TXBERT circuit 11 will be considered in more detail with reference to Fig. 6. The TXBERT circuit 11 has a TXTSSEL component 40. The component 40 is used to generate the transmit enables for the transmit Bert data. It consists of an 8 bit counter formed by the signals CNT0 through to CNT7. This counter is reset by the signal TMO which indicates the start of the transmit multiframe. The signal TMO comes from the Dallas chip 23. It is latched and gated to form signal TS since which directly resets the counter. The output of this counter is then decoded to form a signal TXBERT. This signal goes high during which data is to be transmitted. In unframed mode this signal is patched permanently high. The signal is patched in the CLBTX time slot select. Note that signal TFSYNC directly resets the high five bits of the eight bit counter whereas the low three bits of the counter are set to the value 001 by this signal. This ensures

everything lines up with the timing of the TMO signal.

The output TXBERTS of the TXTSSEL component 41 passes to a TXPRBS component 41. This component 41 is used to generate the transmit PRBS Bert pattern. It consists of a 15 bit shift register formed by signals TAP0 through to TAP14. Various outputs from this shift register are then gated together and fed back to the input of shift register to generate a PRBS pattern. The CLBTXPRBS select is patched to select which taps are enabled. The CLB map TX polarity select is patched to determine the polarity of the transmitted PRBS data. Signal INJER is controlled by the V40 14. When this signal toggles high during the transmission of Bert data a bit error is injected into the transmitted data stream. This bit error signal is decoded to signal BERR which inverts the output of the PRBS shift register. Note the output of the shift register occurs from the eighth tap signal TAP7 although it could have come from any of the other taps if desired.

The TXJITTER circuit 13 will now be described with reference to Fig. 7. It has a TXCKEN component 50. This component 50 is used to generate the transmit clock. The transmit clock can be jittered under the influence of signals DOJIT and JMOD1. When signal DOJIT is high a twelfth of a unit interval phase hit is introduced into the transmit click if a polarity

depending the state of signal JMOD1. These phase hit insertion happen during the time when the line is not marking except in high jitter situations.

Fig. 7 also shows a TXHDB3 component 42. This component 42 is used to encode the transmit data in a HDB3 format. Note it can be patched so that the transmit data is AMI. The configuration must do this encoding as the Dallas chip 23 can only encode for HDB3 during unframed transmission when the HDB3 coding is needed. For this reason the Dallas transmitter is always used to transmit AMI data. The CLB maps TX line code and TX framing are patched to enable AMI mode. In this mode, no extra violations are inserted into the transmit data.

Fig. 7 also shows a GRADREGO component 51. This component 51 contains the circuitry which is used to set the frequency of the transmitted jitter. It consists of a nineteen bit counter which is formed by signals JCNT(0:19) together with registers which are used to compare against this count value. The output INCAMP indicates when it is time to inject a twelfth of a unit jitter hit into the transmitted jitter waveform. The block EXTRACLK also enables fine tuning of the jitter frequency. The output INCAMP of the component 51 passes to an AMPREG component 52.

The component 51 is used to set the amplitude of

the transmitted jitter. It consists of an eight bit latch which the V40 14 can write to and an eight bit counter which is compared to the contents of this latch to indicate when the required jitter amplitude has been reached.

The INCAMP signal also passes to a JITGEN component 57. This component is used to control the generation of transmit jitter in the TX jitter generation circuitry.

It can be seen from the above discussion of Figs. 3 to 7 that the embodiment of Fig. 1 makes use primarily of digital components. This makes embodiments of the present invention easier and cheaper to produce. In the embodiment of Fig. 1, the PLL circuit 103 needs to be an analog circuit, but the fact that the PLL circuit 103 has a low time constant means that it is easy to produce and is thus inexpensive.

In the above discussion, it is assumed that the pulse-train received at input 100 is a co-directional digital data signal, in which the clock information and data are included together in one signal. The present invention may also be applied to clock signals which are not included with data, clocks still being recovered in the same way as discussed above. Moreover, the present invention may be used to investigate the jitter of an analog signal, by converting that to a digital signal before being input to input 100.

CLAIMS

1. A method of measuring jitter in a digital signal comprising:

forming an offset reference clock signal (101, 102, 103), being offset by a predetermined frequency amount from said digital signal;

sampling (110) said digital signal at sampling times determined by said offset reference clock signal, such that, in the absence of jitter and said offset by a predetermined frequency, there are a predetermined number of sampling times in each bit of said digital signal;

detecting (113, 114) occasions when the number of sampling times in any bit of said digital signal is different from said predetermined number;

counting (119) said occasions over a predetermined time; and

deriving (121) at least one measure of jitter from said counting of said occasions.

2. A method according to claim 1, wherein said offset reference clock signal is formed by extracting (101) a clock signal from said digital signal and offsetting (102) said clock signal by said predetermined frequency.

3. A method according to claim 2, further including smoothing (103) said offset reference clock signal.

4. A method according to any one of said preceding claims, wherein said sampling times are determined by an integer multiple of the frequency of said offset reference clock signal.

5. A method according to claim 4, wherein said sampling the times are at clock bit intervals being plus and minus one of said integer multiple.

6. A method according to any one of the preceding claims, wherein the predetermined time is inversely proportional to the product of the bit rate of the digital signal and the predetermined frequency amount.

7. A method according to any one of the preceding claims, wherein one of said at least one measure of jitter is obtained by counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and determining the difference between the maximum count value and the minimum count value.

8. A method according to any one of the preceding claims, wherein one of said at least one measure of

jitter is obtained by counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and determining the time difference between the first occasion of the maximum count value and the last occasion of the minimum count value.

9. A method according to claim 8 as dependent on claim 4, wherein the time difference is divided by said integer multiple and said predetermined time.

10. An apparatus for measuring jitter in a digital signal comprising:

means (101, 102, 103) for forming an offset reference clock signal, which clock signal is offset by a predetermined frequency amount from said digital signal;

means (110) for sampling said digital signal at sampling times determined by said offset reference clock signal, such that, in the absence of jitter and said offset by a predetermined frequency, there are a predetermined number of sampling times in each bit of said digital signal;

means (112, 114) for detecting occasions when the number of sampling times in any bit of said digital

signal is different from said predetermined number; and

means (119) for counting said occasions over a predetermined time, and

means (121) for deriving at least one measure of jitter from said means for counting of said occasions.

11. An apparatus according to claim 10, wherein said means for forming said offset reference clock signal comprises means (102) for extracting a clock signal from said digital signal and means (102) for offsetting the clock signal by said predetermined frequency.

12. An apparatus according to claim 11, wherein said means for forming said offset reference clock signal includes means (103) for smoothing said offset reference clock signal.

13. An apparatus according to any one of claims 10 to 12, wherein said means (121) for deriving one of said at least one measure of jitter comprises means for counting up one value for each of said occasions representing sampling times greater than said predetermined number within a bit and for counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and means for determining the difference between the maximum count

value and the minimum count value.

14. An apparatus according to any one of claims 10 to 12, wherein said means (101) for deriving one of said at least one measure of jitter comprises means for counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit and for counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and means for determining the time difference between the first occasion of the maximum count value and the last occasion of the minimum count value.

15. An apparatus for measuring jitter in a digital signal comprising:

an offset unit (101, 102, 103) arranged to form an offset reference clock signal, being offset by a predetermined frequency amount from said digital signal;

a sampler (110) arranged to sample said digital signal at sampling times determined by said offset reference clock signal such that, in the absence of jitter and said offset by a predetermined frequency, there are a predetermined number of sampling times in each bit of said digital signal;

at least one detector (113, 114) arranged to detect

occasions when the number of sampling times in any bit of said digital signal is different from said predetermined number;

a counter (119) arranged to count said occasions over a predetermined time, and

an analyser (121) arranged to derive at least one measure of jitter from said counting of said occasions.

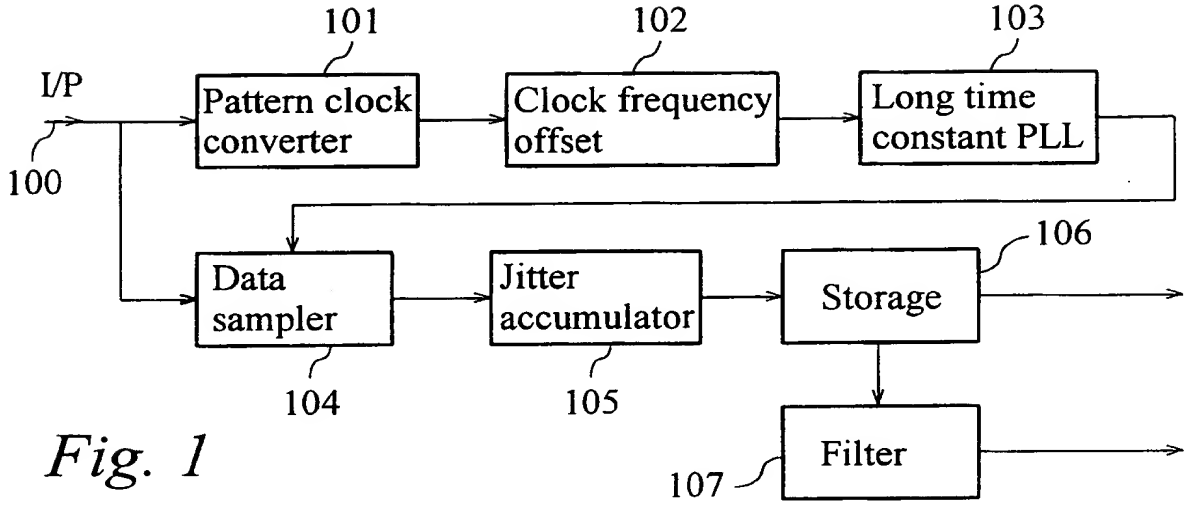
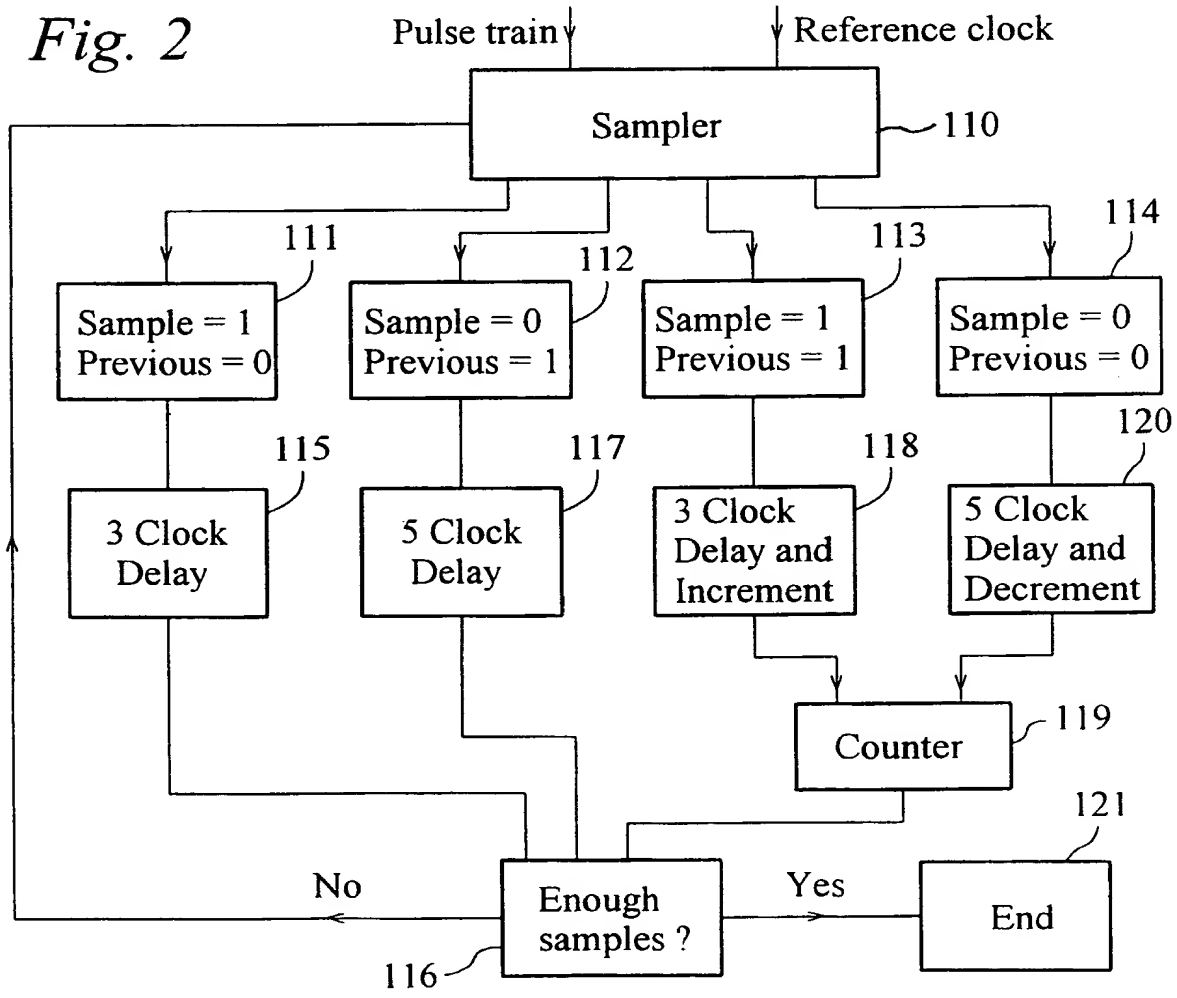

101
102
103
I/P
Pattern clock converter
Clock frequency offset
Long time constant PLL
100
106
Data sampler
Jitter accumulator
Storage
104
105
Filter
107

Fig. 1

Fig. 2


Pulse train
Reference clock
Sampler
110
111
112
113
114
Sample = 1 Previous = 0
Sample = 0 Previous = 1
Sample = 1 Previous = 1
Sample = 0 Previous = 0
115
117
118
120
3 Clock Delay
5 Clock Delay
3 Clock Delay and Increment
5 Clock Delay and Decrement
Counter
119
121
No
Enough samples ?
Yes
End
116

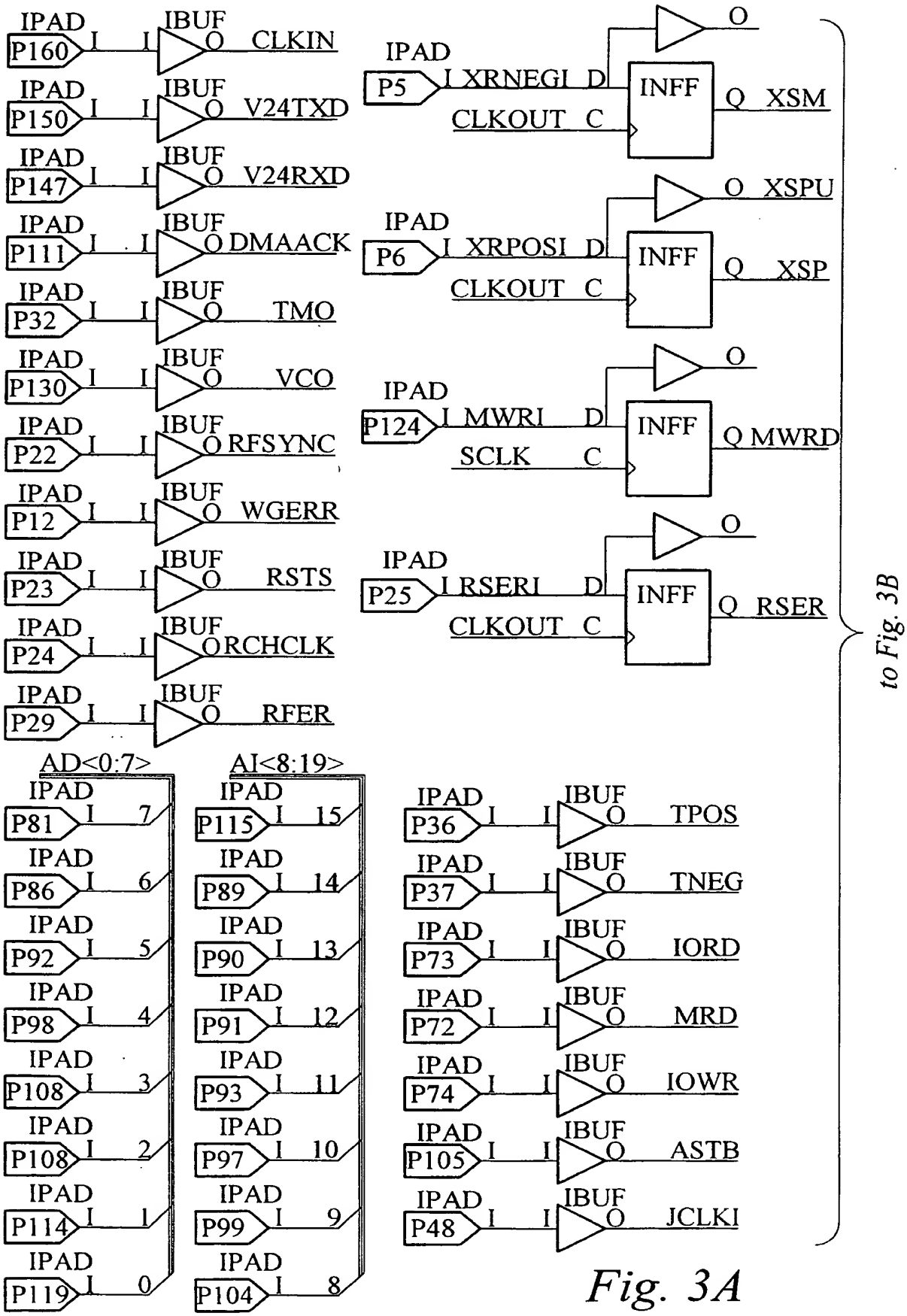

IPAD P160 I IBUF I O CLKIN
IPAD P150 I IBUF I O V24TXD
IPAD P147 I IBUF I O V24RXD
IPAD P111 I IBUF I O DMAACK
IPAD P32 I IBUF I O TMO
IPAD P130 I IBUF I O VCO
IPAD P22 I IBUF I O RFSYNC
IPAD P12 I IBUF I O WGERR
IPAD P23 I IBUF I O RSTS
IPAD P24 I IBUF I O RCHCLK
IPAD P29 I IBUF I O RFER
IPAD P5 I XRNEGI D INFF Q XSM
CLKOUT C
IPAD P6 I XRPOSI D INFF Q XSP
CLKOUT C
IPAD P124 I MWRI D INFF Q MWRD
SCLK C
IPAD P25 I RSERI D INFF Q RSER
CLKOUT C
O
AD<0:7>
AI<8:19>
IPAD P81 I 7
IPAD P86 I 6
IPAD P92 I 5
IPAD P98 I 4
IPAD P108 I 3
IPAD P108 I 2
IPAD P114 I 1
IPAD P119 I 0
IPAD P115 I 15
IPAD P89 I 14
IPAD P90 I 13
IPAD P91 I 12
IPAD P93 I 11
IPAD P97 I 10
IPAD P99 I 9
IPAD P104 I 8
IPAD P36 I IBUF I O TPOS
IPAD P37 I IBUF I O TNEG
IPAD P73 I IBUF I O IORD
IPAD P72 I IBUF I O MRD
IPAD P74 I IBUF I O IOWR
IPAD P105 I IBUF I O ASTB
IPAD P48 I IBUF I O JCLKI
to Fig. 3B

Fig. 3A

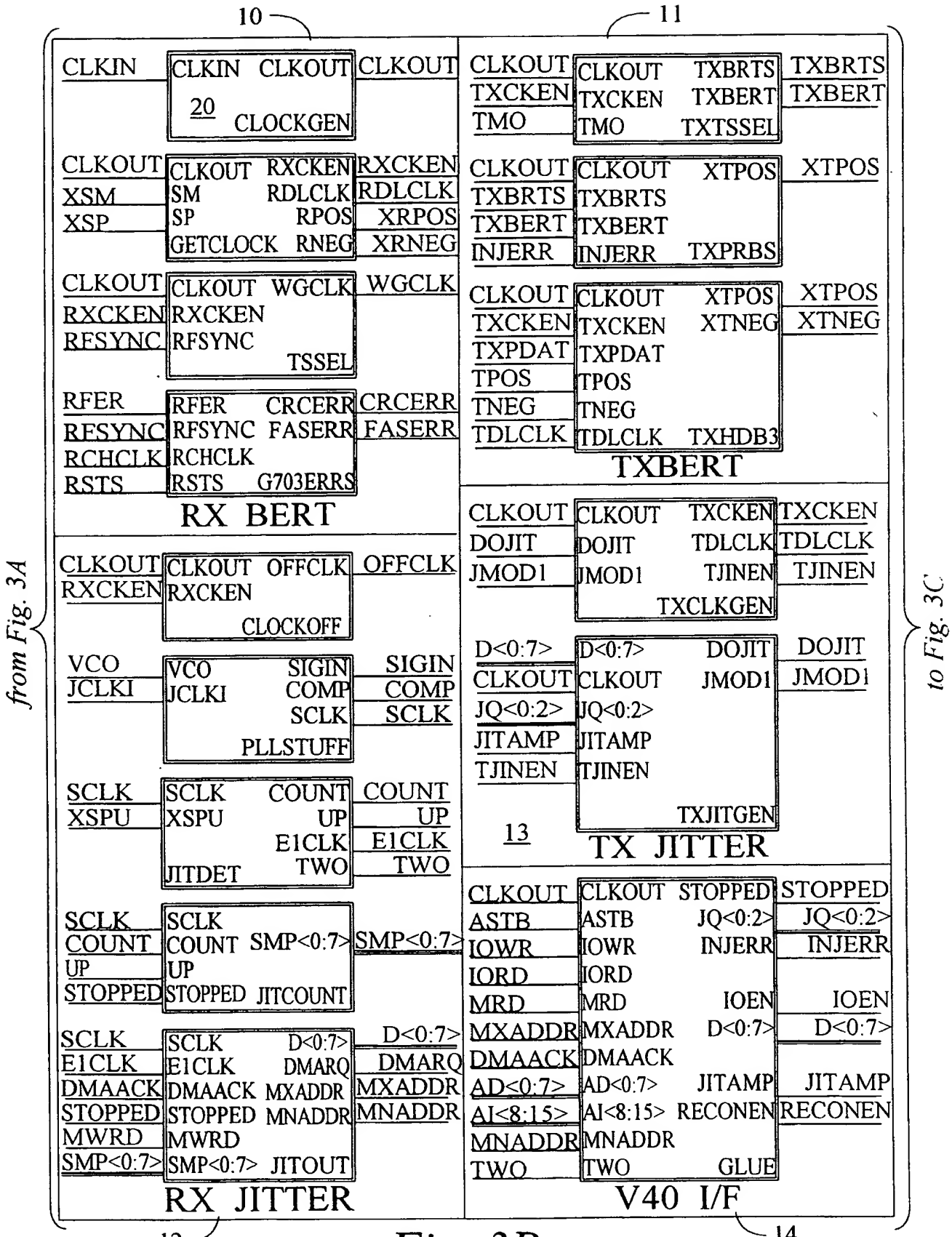

10
11
CLKIN
CLKIN CLKOUT
CLKOUT
20
CLOCKGEN
CLKOUT
XSM
XSP
CLKOUT RXCKEN
SM RDLCLK
SP RPOS
GETCLOCK RNEG
RXCKEN
RDLCLK
XRPOS
XRNEG
CLKOUT
RXCKEN
RFSYNC
CLKOUT WGCLK
RXCKEN
RFSYNC
TSSEL
WGCLK
RFER
RFSYNC
RCHCLK
RSTS
RFER CRCERR
RFSYNC FASERR
RCHCLK
RSTS G703ERRS
CRCERR
FASERR
RX BERT
CLKOUT
TXCKEN
TMO
CLKOUT TXBRTS
TXCKEN TXBERT
TMO TXTSSEL
TXBRTS
TXBERT
CLKOUT
TXBRTS
TXBERT
INJERR
CLKOUT XTPOS
TXBRTS
TXBERT
INJERR TXPRBS
XTPOS
CLKOUT
TXCKEN
TXPDAT
TPOS
TNEG
TDLCLK
CLKOUT XTPOS
TXCKEN XTNEG
TXPDAT
TPOS
TNEG
TDLCLK TXHDB3
XTPOS
XTNEG
TXBERT
CLKOUT
DOJIT
JMOD1
CLKOUT TXCKEN
DOJIT TDLCLK
JMOD1 TJINEN
TXCLKGEN
TXCKEN
TDLCLK
TJINEN
D<0:7>
CLKOUT
JQ<0:2>
JITAMP
TJINEN
D<0:7> DOJIT
CLKOUT JMOD1
JQ<0:2>
JITAMP
TJINEN
TXJITGEN
DOJIT
JMOD1
13
TX JITTER
CLKOUT
RXCKEN
CLKOUT OFFCLK
RXCKEN
CLOCKOFF
OFFCLK
VCO
JCLKI
VCO SIGIN
JCLKI COMP
SCLK
PLLSTUFF
SIGIN
COMP
SCLK
SCLK
XSPU
SCLK COUNT
XSPU UP
E1CLK
JITDET TWO
COUNT
UP
E1CLK
TWO
SCLK
COUNT
UP
STOPPED
SCLK
COUNT SMP<0:7>
UP
STOPPED JITCOUNT
SMP<0:7>
SCLK
E1CLK
DMAACK
STOPPED
MWRD
SMP<0:7>
SCLK D<0:7>
E1CLK DMARQ
DMAACK MXADDR
STOPPED MNADDR
MWRD
SMP<0:7> JITOUT
D<0:7>
DMARQ
MXADDR
MNADDR
RX JITTER
12
CLKOUT
ASTB
IOWR
IORD
MRD
MXADDR
DMAACK
AD<0:7>
AI<8:15>
MNADDR
TWO
CLKOUT STOPPED
ASTB JQ<0:2>
IOWR INJERR
IORD
MRD IOEN
MXADDR D<0:7>
DMAACK
AD<0:7> JITAMP
AI<8:15> RECONEN
MNADDR
TWO GLUE
STOPPED
JQ<0:2>
INJERR
IOEN
D<0:7>
JITAMP
RECONEN
V40 I/F
14
from Fig. 3A
to Fig. 3C

Fig. 3B

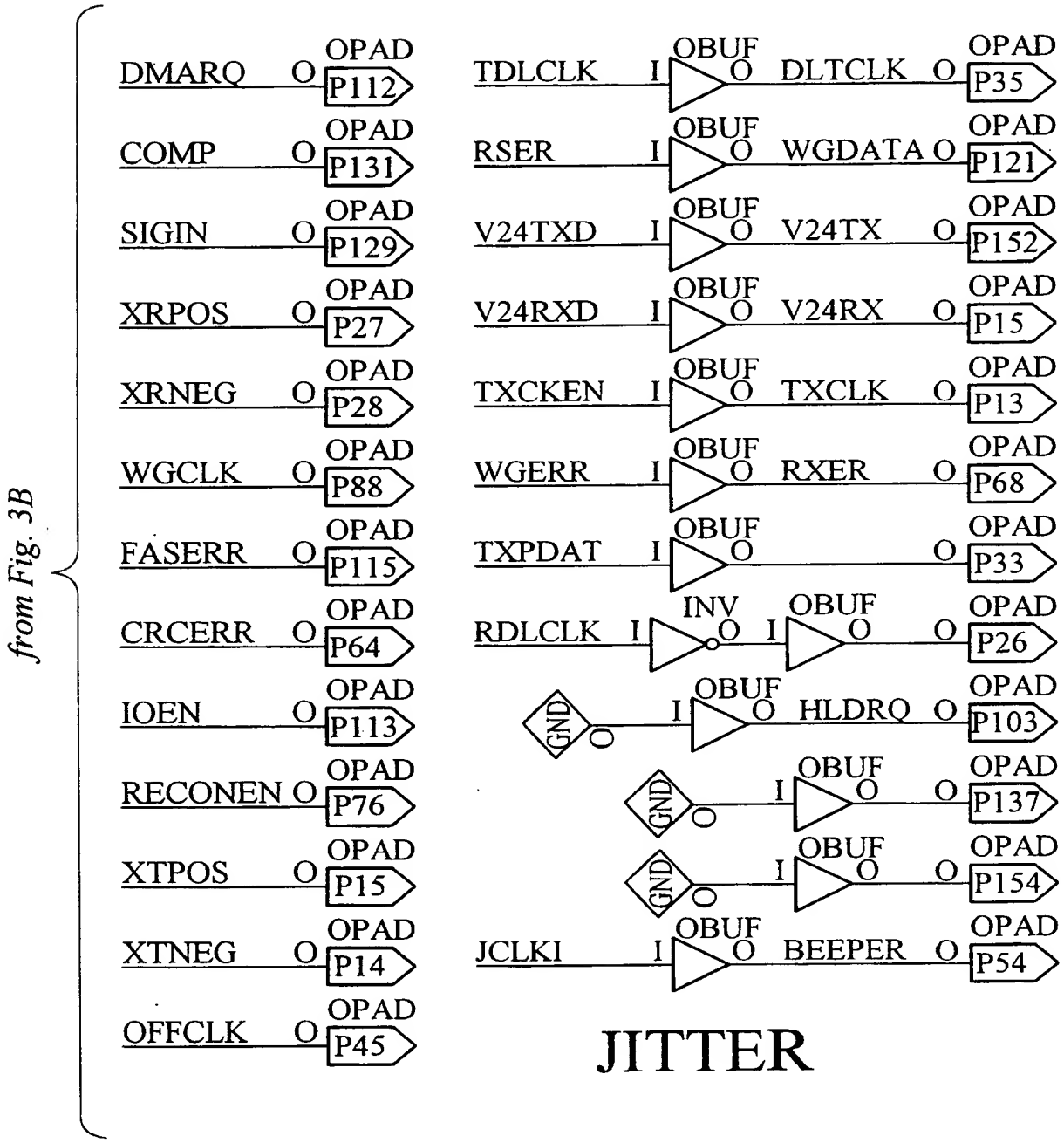

from Fig. 3B
DMARQ O OPAD P112
COMP O OPAD P131
SIGIN O OPAD P129
XRPOS O OPAD P27
XRNEG O OPAD P28
WGCLK O OPAD P88
FASERR O OPAD P115
CRCERR O OPAD P64
IOEN O OPAD P113
RECONEN O OPAD P76
XTPOS O OPAD P15
XTNEG O OPAD P14
OFFCLK O OPAD P45
TDLCLK I OBUF O DLTCLK O OPAD P35
RSER I OBUF O WGDATA O OPAD P121
V24TXD I OBUF O V24TX O OPAD P152
V24RXD I OBUF O V24RX O OPAD P15
TXCKEN I OBUF O TXCLK O OPAD P13
WGERR I OBUF O RXER O OPAD P68
TXPDAT I OBUF O O OPAD P33
RDLCLK I INV O I OBUF O O OPAD P26
GND O I OBUF O HLDRQ O OPAD P103
GND O I OBUF O O OPAD P137
GND O I OBUF O O OPAD P154
JCLKI I OBUF O BEEPER O OPAD P54
JITTER

Fig. 3C

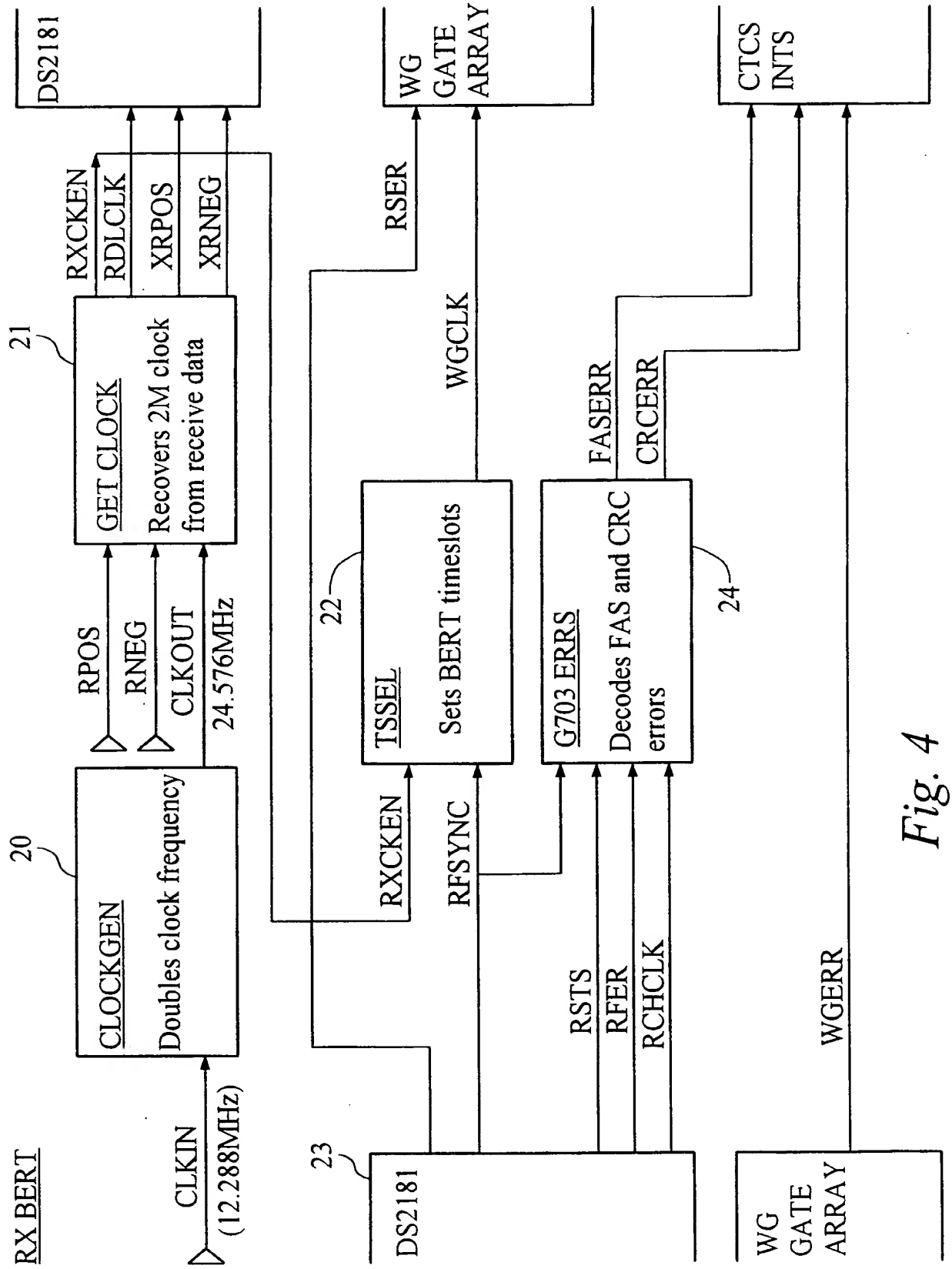

RX BERT
CLKIN
(12.288MHz)
20
CLOCKGEN
Doubles clock frequency
RPOS
RNEG
CLKOUT
24.576MHz
21
GET CLOCK
Recovers 2M clock from receive data
RXCKEN
RDLCLK
XRPOS
XRNEG
DS2181
RXCKEN
RFSYNC
22
TSSEL
Sets BERT timeslots
RSER
WGCLK
WG GATE ARRAY
RSTS
RFER
RCHCLK
23
DS2181
FASERR
CRCERR
24
G703 ERRS
Decodes FAS and CRC errors
CTCS INTS
WGERR
WG GATE ARRAY

Fig. 4

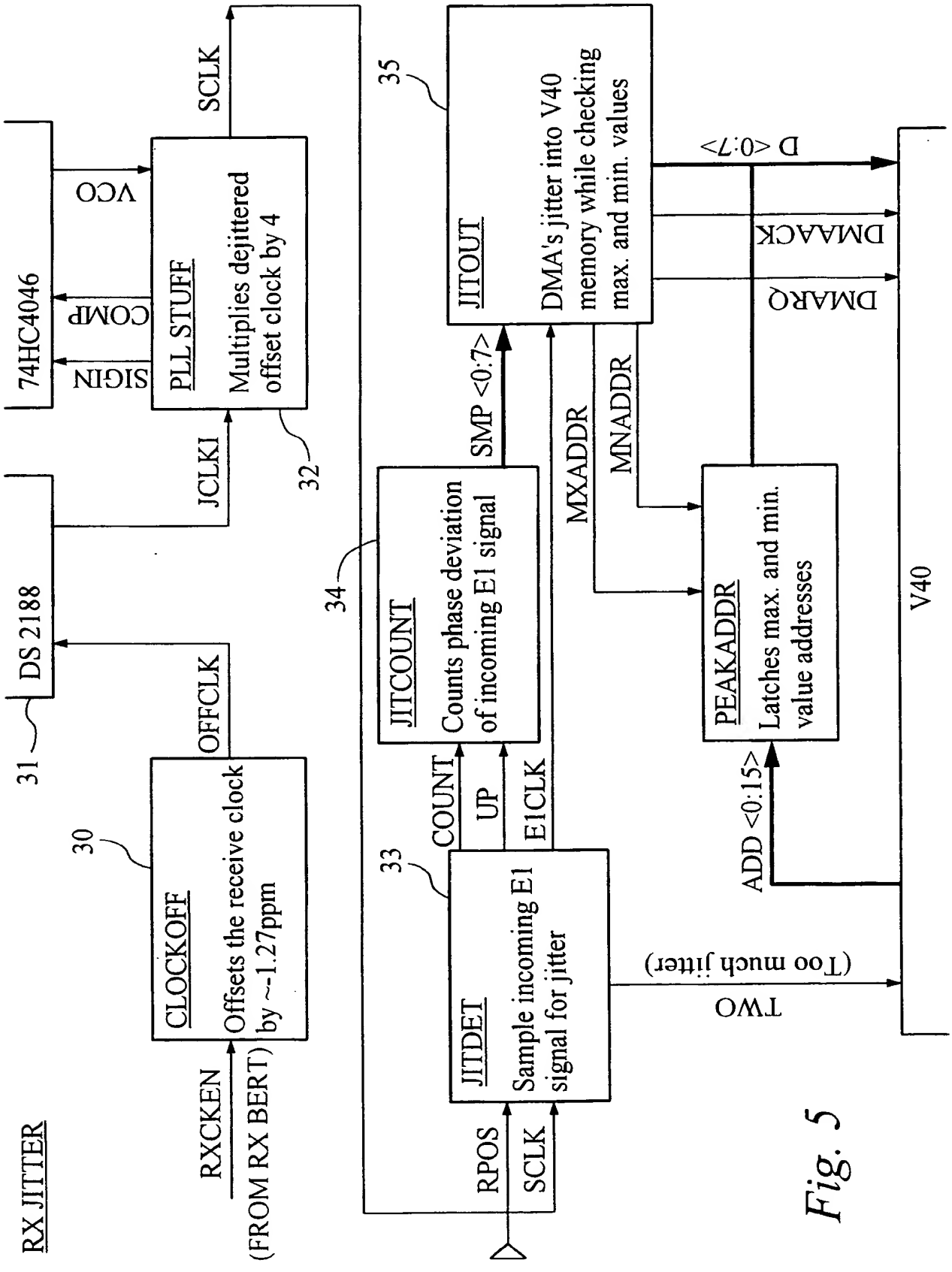

RX JITTER
RXCKEN
(FROM RX BERT)
30
CLOCKOFF
Offsets the receive clock by ~1.27ppm
OFFCLK
31
DS 2188
JCLKI
32
74HC4046
VCO
COMP
SIGIN
PLL STUFF
Multiplies dejittered offset clock by 4
SCLK
34
JITCOUNT
Counts phase deviation of incoming E1 signal
SMP <0:7>
35
JITOUT
DMA's jitter into V40 memory while checking max. and min. values
D <0:7>
DMARQ
DMAACK
MXADDR
MNADDR
33
JITDET
Sample incoming E1 signal for jitter
COUNT
UP
E1CLK
RPOS
SCLK
TWO
(Too much jitter)
PEAKADDR
Latches max. and min. value addresses
ADD <0:15>
V40

Fig. 5

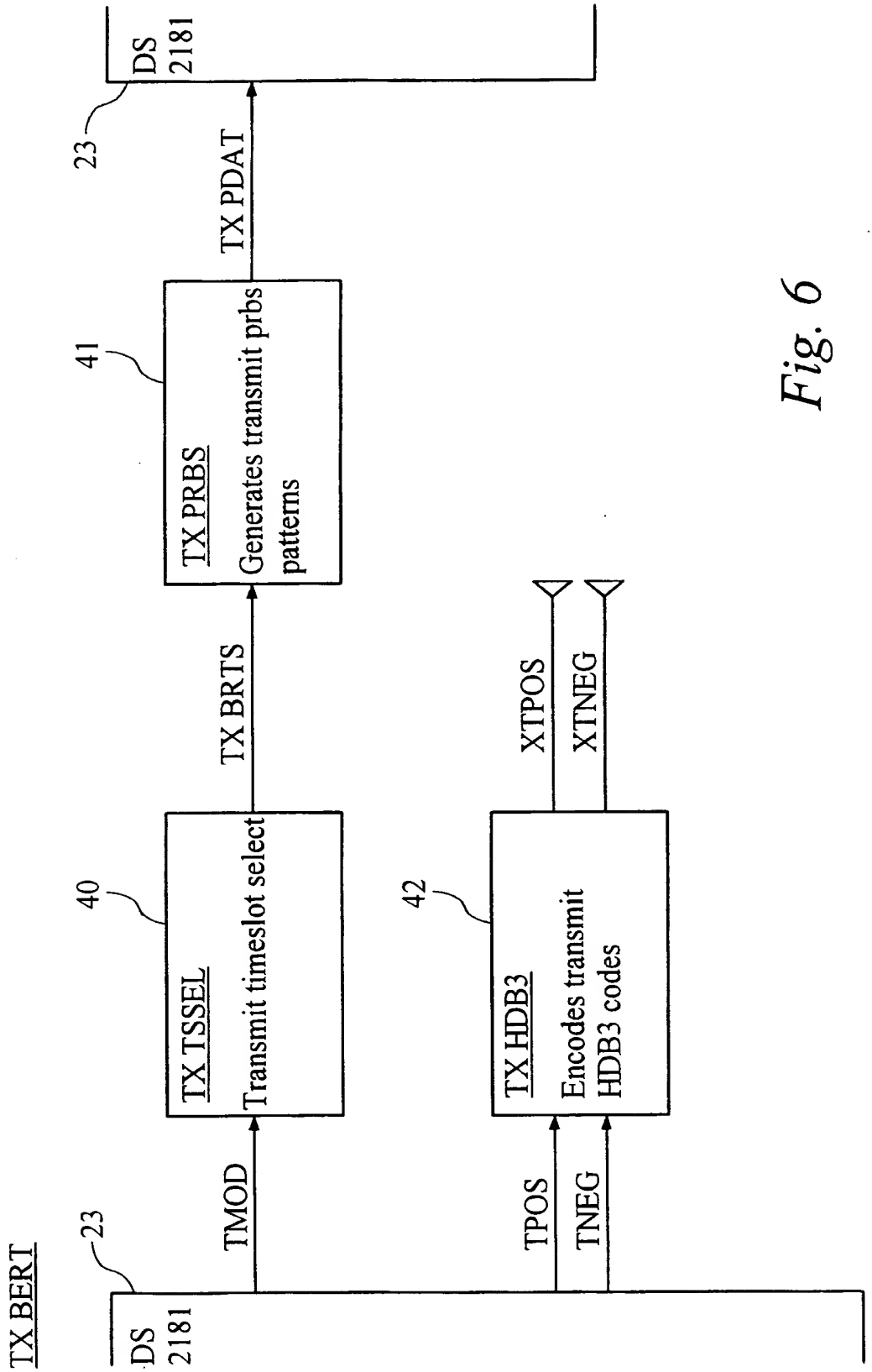

TX BERT
DS 2181
23
TMOD
TPOS
TNEG
40
TX TSSEL
Transmit timeslot select
42
TX HDB3
Encodes transmit HDB3 codes
TX BRTS
XTPOS
XTNEG
41
TX PRBS
Generates transmit prbs patterns
TX PDAT
23
DS 2181

Fig. 6

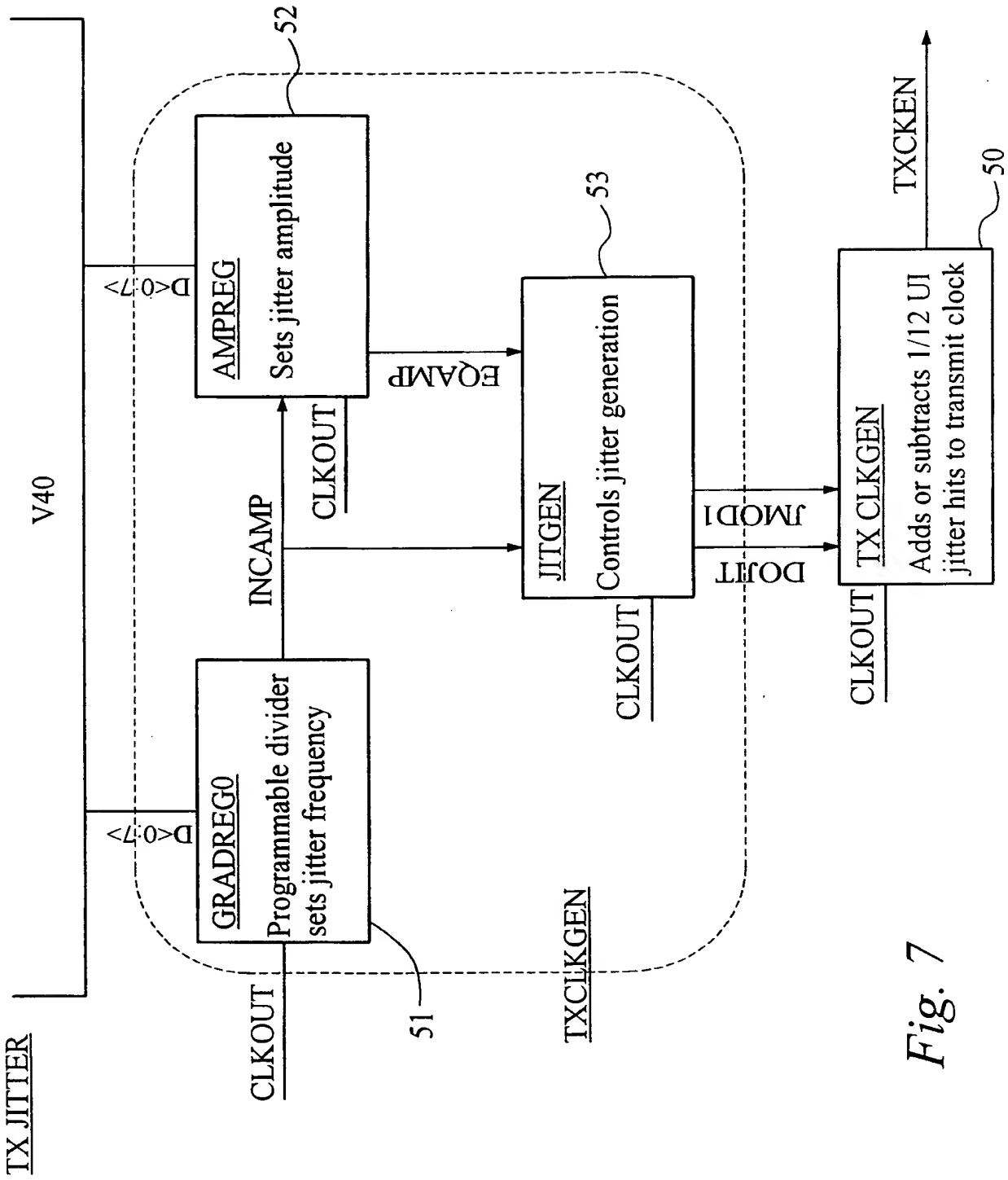

TX JITTER
V40
D<0:7>
AMPREG
Sets jitter amplitude
52
EQAMP
JITGEN
Controls jitter generation
53
DOJIT
JMOD1
TX CLKGEN
Adds or subtracts 1/12 UI jitter hits to transmit clock
50
TXCKEN
CLKOUT
INCAMP
CLKOUT
D<0:7>
GRADREG0
Programmable divider sets jitter frequency
CLKOUT
51
TXCLKGEN

Fig. 7

INTERNATIONAL SEARCH REPORT

national Application No
PCT/GB 99/01339

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L1/20 H04L7/033

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 975 634 A (SHOHET YUVAL) 4 December 1990 (1990-12-04) the whole document	1-15
A	EP 0 362 491 A (WANDEL & GOLTERMANN) 11 April 1990 (1990-04-11) the whole document	1-15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

' Special categories of cited documents :

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 July 1999	04/08/1999

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 99/01339

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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EP 0362491 A	11-04-1990	DE 3833486 C	03-08-1989
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		US 4974234 A	27-11-1990